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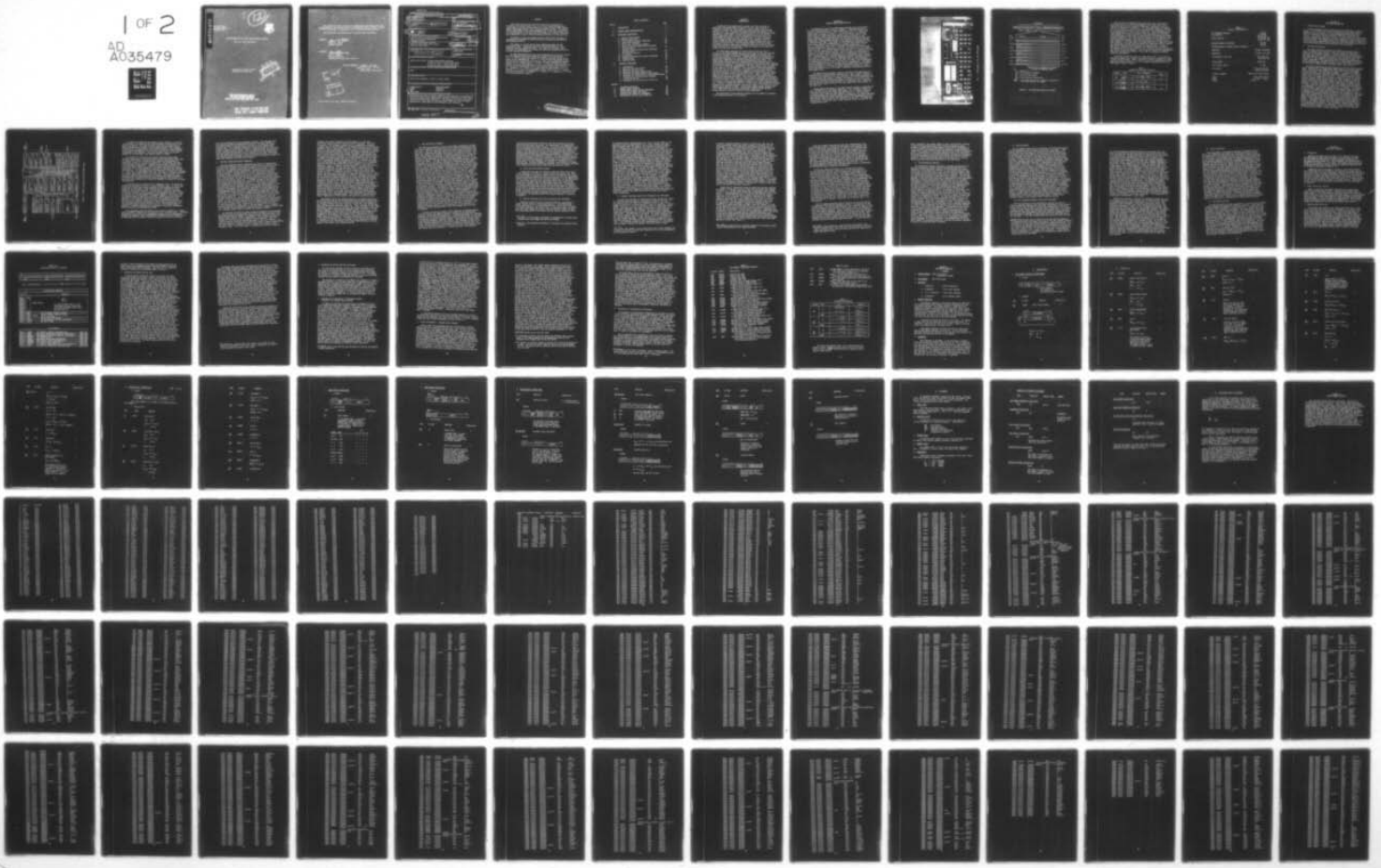

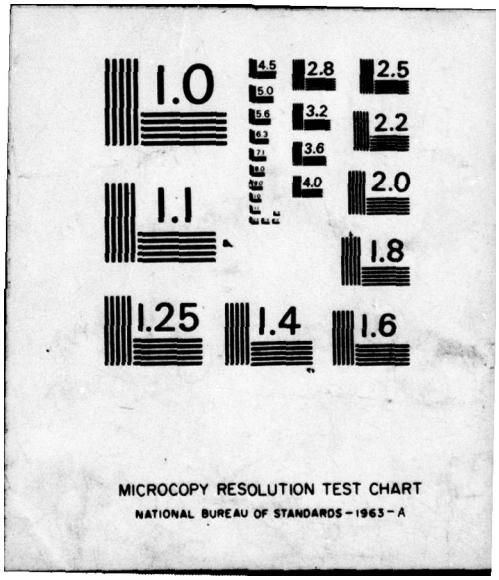
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RADC-TR-76-362
Technical Report
December 1976

A MODEM/CONTROLLER FOR TDMA COMMUNICATIONS SYSTEMS

The Ohio State Univerasity

ROME AIR DEVELOPMENT CENTER
AIR FORCE SYSTEMS COMMAND
GRIFFISS AIR FORCE BASE, NEW YORK 13441

This report has been reviewed by the RADC Information Office (OI) and is releasable to the National Technical Information Service (NTIS). At NTIS it will be releasable to the general public including foreign nations.

This report has been reviewed and is approved for publication.

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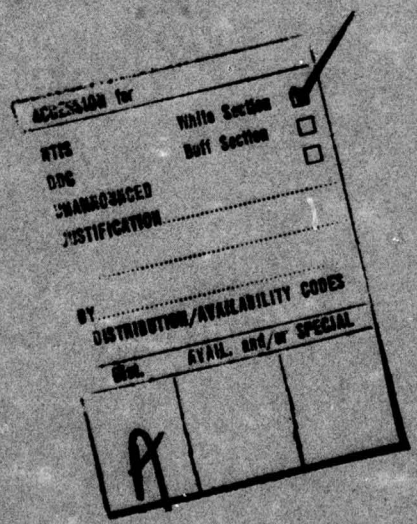

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This report discusses the design, operation, and capability of prototype Time Division Multiple Access (TDMA) modems developed for RADC by the Ohio State University Electroscience Laboratory. The applicable acceptance test procedures and both bench and link test data which demonstrate that the modems operate with a high degree of effectiveness is also presented.

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PREFACE

This report contains the functional description, operating instructions, and test procedures for a set of four modems designed and constructed at the Ohio State University for the Air Force Sytems Command, Rome Air Development Center, under Contract F30602-72-C-0162. The devices differ significantly from other implementations in that the transmissions are timed precisely at the satellite with respect to a network clock which may be generated at any of the participating stations or at the satellite.

In addition to the usual modem functions, such control functions as requesting and assignment of data slots and I/O devices are performed by the modem/controllers.

This report is a first version of an operations manual for the modem/controllers. The devices are being tested operationally under a successor contract, F30602-75-C-0061. As a result of the tests, modifications and improvements may be made and additional documents pertaining to their use may be generated.

The TDMA modem/controllers have been developed over a period of several years by a project staff whose composition changes from time to time. Dr. R. J. Huff developed the concept and directed and participated in all phases of the implementation. Mr. R. C. Taylor oversaw the package design and fabrication, coordinated the technical staff, and assembled the present report. Mr. T. Treadway and Mr. S. Talbot of RADC contributed by their technical interest and suggestions as well as by general contract monitoring. We also wish to acknowledge the many contributions made by the following: K. L. Reinhard, T. W. Miller, D. C. Upp (Technique Development); Dr. J. D. McMillen, J. D. Clover (non-programmable digital logic); Dr. D. E. Svoboda (digital controller); M. D. Gordon, W. L. Hensley, C. H. Boehnker, F. S. Cook, D. E. Henry (technical support).

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SECTION I
INTRODUCTION

In TDMA satellite communication systems, the time continuum is subdivided into nonoverlapping intervals or slots, each of which is (normally) allocated for the relaying of signals from no more than one terminal at a time. The slots are normally defined with respect to the time base of a signal present on the satellite down link designated as the network clock signal (NCS). At each user terminal, the time base of a locally-generated signal (clock) is aligned with the time base of the received NCS to establish a local receive clock. In turn, a transmit clock is timed so that pulses transmitted by the terminal during intervals identified from the transmit clock occupy assigned time slots on arriving at the satellite. The information needed to maintain proper transmitter timing is obtained by estimating the error in arrival time of pulses transmitted by the terminal as they are received on the down-link relative to the local receive clock.

The TDMA modems developed at The Ohio State University rely on the use of two coupled sampled-data delay-lock loops at each user terminal to maintain the desired timing relationships between the transmit and receive clock signals and the NCS. Baseband waveforms having appropriate correlation properties, e.g., pseudo-noise (PN) codes, are impressed as digital phase modulation on each pulse processed by those loops. The synchronizing loops maintain the transmit and receive timing errors at values which are small relative to the duration of the symbols which comprise the modulation waveforms. Consequently, the local receive clock at a terminal can be used to time the demodulation of all data-carrying pulses present on the down-link to that terminal. This approach to timing the demodulator, coupled with the use of differential detection to extract data from the data-carrying burst, allows using a preamble at the beginning of each burst which has a duration of only one data bit length. Thus, a relatively small number of data bits can be conveyed within a slot without significantly compromising signaling efficiency. This feature has considerable advantages in systems containing small terminals which request assignments and establish links in real time. In such systems, the spectra of the data-carrying signals are spread using appropriate waveforms ("codes") by at least a moderate factor, e.g., sixteen, to reduce the effects of unintentional interference and multipath propagation on system performance; the spectral widths of the timing and data signals would normally be equal. Unlike other communications systems, the O.S.U. TDMA system uses accurate transmitter timing to permit multiple message detection using one relatively simple demodulator.

The description of and operating procedure for the modems is contained in the remaining sections of this manual.

SECTION II
GENERAL MODEM CHARACTERISTICS

A photograph of one of the TDMA modems developed and constructed at The Ohio State University is shown in Figure 1. The modem can be configured to establish either a lower-rate format (LRF) or a higher-rate format (HRF), as shown in Figure 2. To utilize the LRF, the received signal power to single-sided noise density ratio (P_r/N_o, P_r/kT in the case of thermal noise) associated with the smallest terminal in the network must equal or exceed 51 dB-Hz and the satellite channel must have a bandwidth of approximately 500 KHz. The respective values for the HRF are 60 dB-Hz and 4 MHz. Each modem can simultaneously accommodate an I/O device which operates asynchronously at an average data rate of 75 bps, e.g., a teleprinter, and a device which operates synchronously at a 2400 bps average data rate, e.g., a vocoder. The 2400 bps device can be operated either in a shared-channel push-to-talk mode or in a full duplex mode. Two-way communications between 75 bps devices is accomplished through sharing of a single simplex channel. When the modems are configured to establish the HRF, data is transmitted at an instantaneous rate of 87.6 Kbps. Pseudo-noise (PN) codes are employed to spread the signal spectrum by a factor of sixteen to provide a moderate amount of protection against multipath and interference. In the LRF mode, the data are conveyed at an instantaneous rate of either 10.95 Kbps or 87.6 Kbps; the corresponding spectrum spreading factors are sixteen and two, respectively. The modems can be configured in either a two-phase mode, wherein each signal pulse is biphase modulated by a PN code to effect spectrum spreading, or a four-phase mode wherein a pair of PN codes is employed to quadraphase modulate each signal pulse.

The TDMA signaling format is defined relative to the time base of a pulsed-envelope, phase-modulated network clock signal (Figure 2) which is relayed by the satellite to all user terminals. That signal originates at a predesignated user terminal, however, the network clock transmission function can be transferred from one terminal to another in real time under operator control with minimal disruption of established links. When suitable satellites become available, the clock signal may also originate at the satellite.

Approximately one-fourth of the TDMA signaling format is allocated for use in performing all "overhead" operations. The "overhead" signals include one NCS, one control signal per network control terminal, and one link/range (L/R) signal per user terminal (Figure 2). The allocation of three overhead slot triplets (three LLL assignments) for use by terminals which perform network control functions permits the accommodation of up to 380 terminals with the HRF and 44 terminals with the LRF. The remaining three-fourths of the time slots in the signaling format are used for the transmission of data.

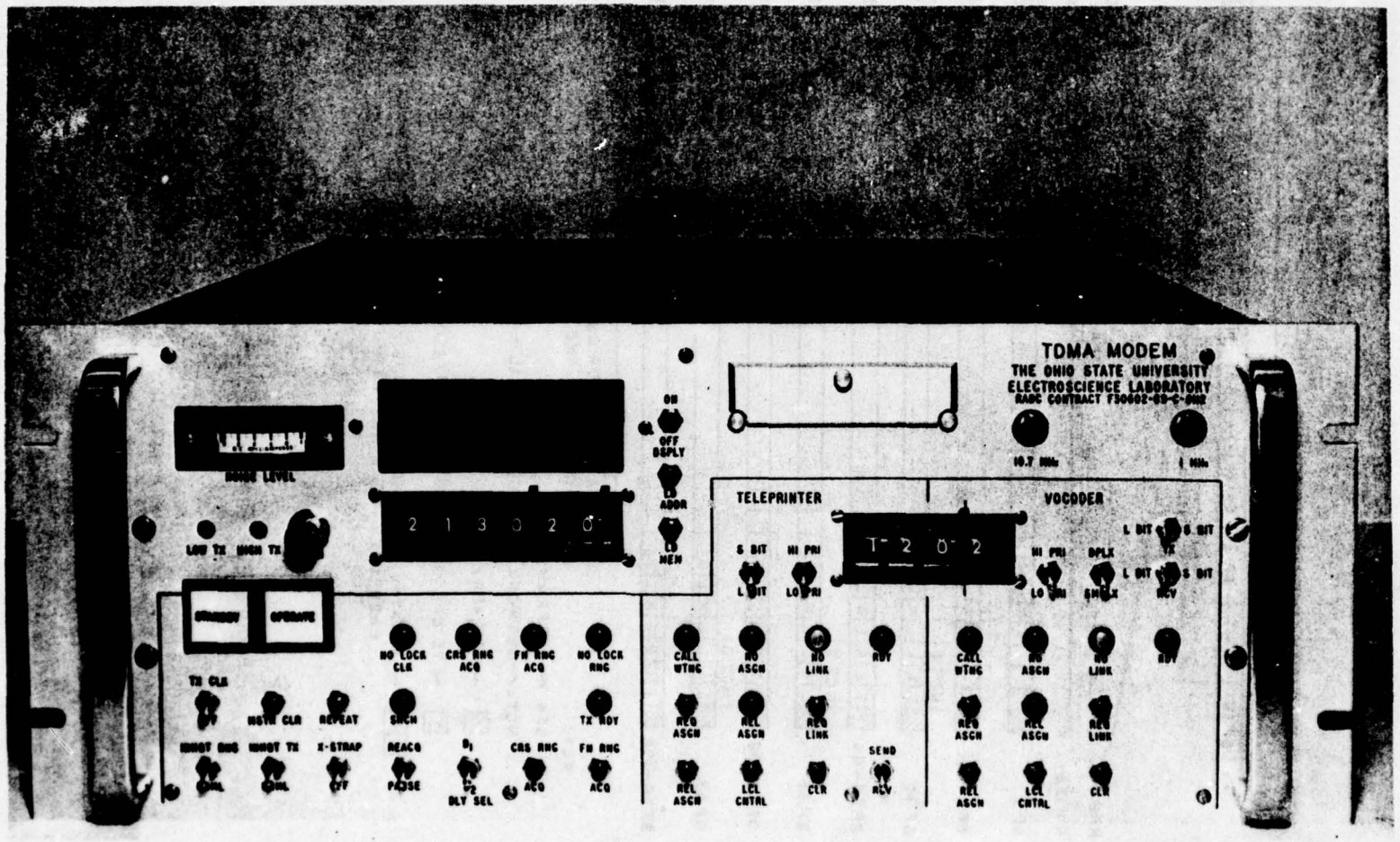

Fig. 1. Photograph of the OSU TDMA modem.

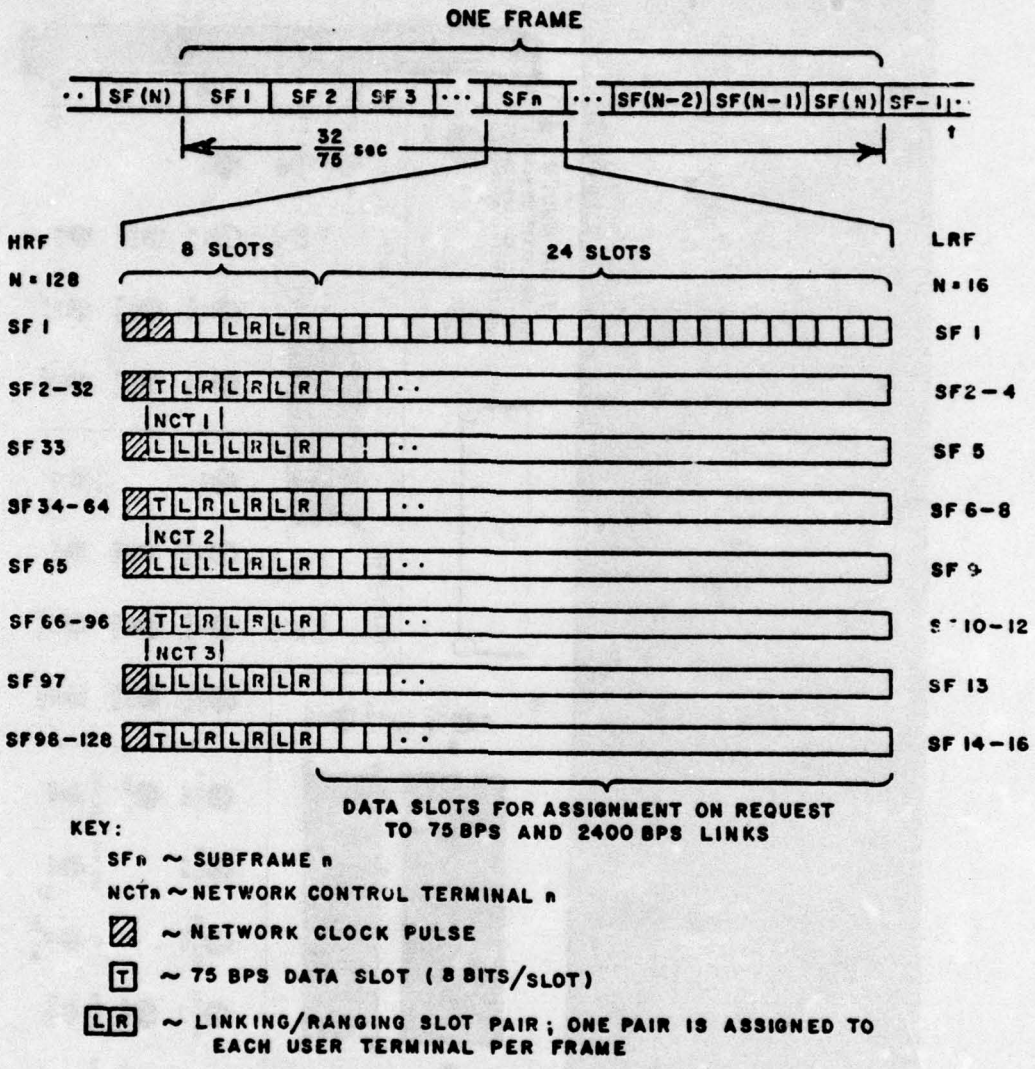

Figure 2. The TDMA modem signaling formats.

When the LRF is established and a given data slot is employed to convey data at the 87.6 Kbps instantaneous (burst) data rate, sixty-four data symbols can be conveyed in that slot. Otherwise, eight data symbols are conveyed in a data slot. A time-ordered channel is composed of a set of data slots which collectively permit the transmission of data at an average rate of either 75 bps or 2400 bps. Each available type of time-ordered channel can be characterized by the number of consecutive slots spanned by a single burst of the data-carrying waveform, the number of slots contained in one period of that waveform, and the number of data symbols conveyed per slot. Each 2400 bps channel can be subdivided into thirty-two 75 bps channels which can be allocated to a multiplicity of user terminals. Similarly, each 10.95 Kbps burst-rate or longer bit length (LBL) channel can be subdivided into eight 87.6 Kbps burst-rate or shorter bit length (SBL) channels when the LRF is being utilized. In fact a 2400 bps LBL channel can be subdivided into combinations of 2400 bps SBL channels and 75 bps LBL channels, e.g., into four 2400 bps SBL channels and sixteen 75 bps LBL channels. This flexibility permits the management of data slot allocation/utilization in real time to accommodate changing signaling requirements.

An entire net must be set up as either HRF or LRF. In the LRF configuration communication channels may operate either with short bit length or with long bit length. Table I shows the available combinations of communication channel resources. A list of general characteristics of the TDMA modem is shown in Table II.

TABLE I
Communication Channel Resources

Format	Rate	No. of Channels	N_{max}
HRF	75	31 + (768 - 32N)	24
	2400	N	
LRF-LBL	75	3 + (96 - 32N)	3
	2400	N	
LRF-SBL	75	24 + (768 - 32N)	24
	2400	N	

TABLE II
General Characteristics

IF interface frequency	70 MHz
RF bandwidth	4 MHz HRF 500 KHz LRF
P_r/N_o required	51 dB Min. LRF 60 dB Min. HRF
Maximum number of terminals	380 HRF 44 LRF
Maximum number of network control terminals	3
Operation	Demand assignment
Modulation	2ϕ DPSK or 4ϕ DPSK
Instantaneous data rate	87.6 Kbps HRF 10.95 Kbps LRF
Frame length	32/75 sec.
AFC tracking range	$\pm$1 KHz
I/O devices	75 bps teleprinter 2400 bps vocoder
Interval computer	2048-16 bit instructions
Power	480 w/120 v 60 Hz
Size	19" rack 7" panel
Weight	72 lbs.

SECTION III
FUNCTIONAL DESCRIPTION

1. General Block Diagram

A block diagram of The Ohio State University TDMA modem is shown in Figure 3. The transmit and receive subsystems interface with external devices at an IF of 70 MHz. A 75 bps asynchronous-data-buffer and a 2400 bps synchronous-data buffer provide interfaces to external I/O devices. The external computer interface is used primarily to complete data transfers between the modem and an external computer at network control terminal facilities. The numbers shown on the individual blocks in Figure 3 indicate the drawing number where a detailed circuit description may be found. The drawings have been furnished separately from this report.

2. The Digital Controller

The signal processing operations performed by the modem during a time slot depend on the location of that slot within the signaling format and on the modem's status. A digital controller contained within the modem (see Figure 3) exercises control over the various subsystems so that they operate in appropriate states at each instant in time. The controller is also employed to manage and/or process data generated by several subsystems. This approach results in a large number of functions being performed under program (software) control which would otherwise be performed by numerous special-purpose digital logic circuits.

The digital controller has been designed so that the control program can be stored either in random-access memory (RAM) or read-only memory (ROM). Read-only control memories are contained in two of the modems delivered to RADC. The remaining two modems -- including one modem retained at Ohio State for use under a successive contract -- are instrumented with solid-state (volatile) RAM's. The control memories in these latter units are loaded from an external computer by way of the modem/external-computer interface (see Figure 3). This interface is also employed to perform I/O transfers between the modem and the external computer which executes the network control algorithm at a network control terminal. In either configuration, the control memory provides storage for 2048 sixteen-bit instructions; expansion to 4096 words of storage can be accommodated. A twelve-bit program counter is provided. Information subject to manipulation by the controller's arithmetic-logic unit (ALU) is stored in a random access data memory which has a capacity of 256 sixteen-bit words. On application of power to the controller or depression of the MSTR CLR momentary switch (see Figure 1), the contents of the low-order 256 locations of the control memory are transferred to the data memory; the program counter is then set to zero and controller operation enabled. Those operations are performed automatically under hardware control. Peripheral hardware within the modem allows the contents of an arbitrary data memory location to be displayed or altered under control if an appropriate subroutine is contained in the control program. That hardware includes a numeric (octal) display, an octal switch register, and appropriate interface circuits (see Figure 1).

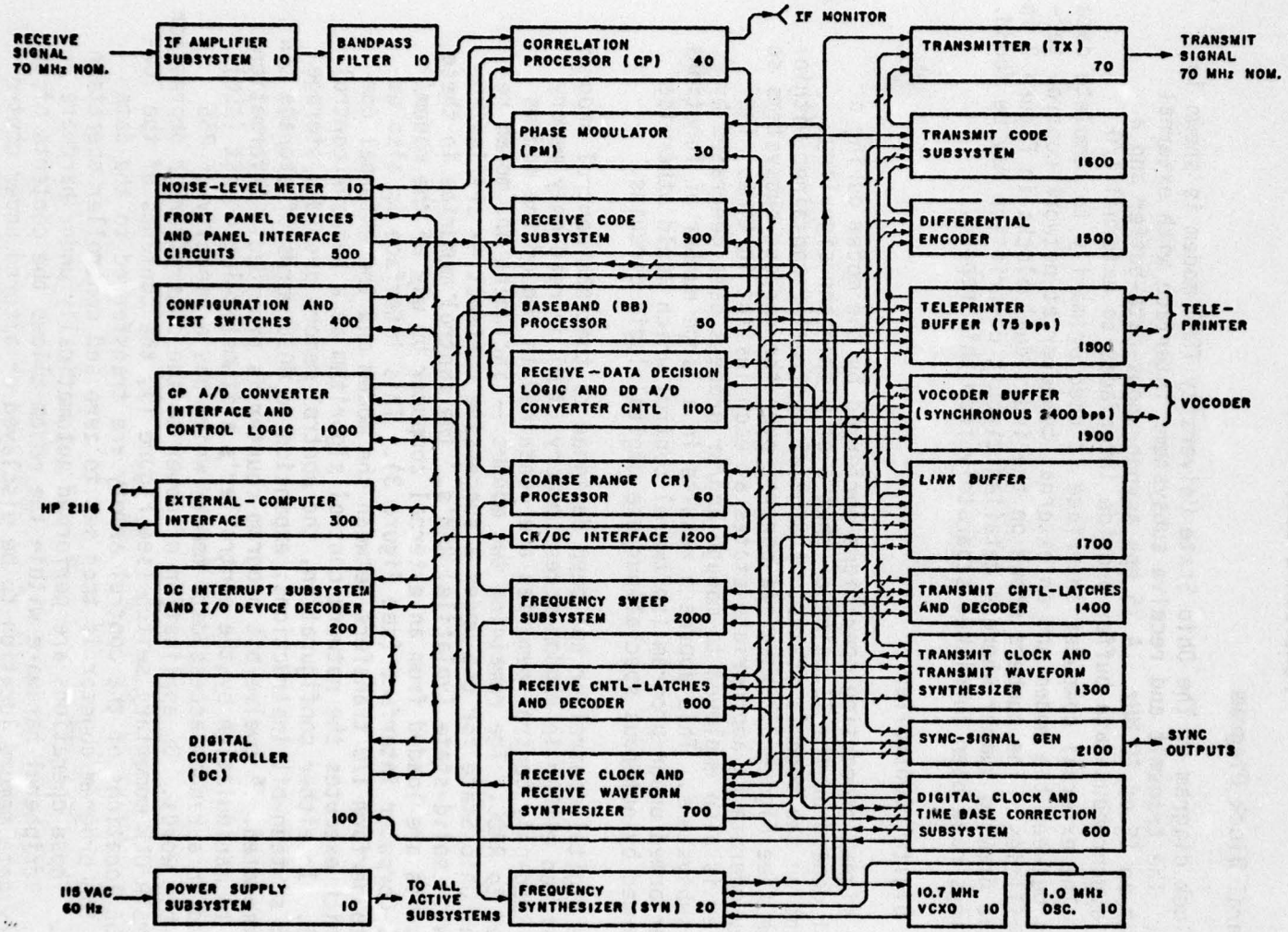

Figure 3. Block diagram of the OSU TDMA modem.

A sixteen-bit accumulator designated as the X register, a (one-bit) carry register, and three four-bit index registers are contained in the digital controller. The index registers are used to generate control memory and data memory addresses under program control. When indexing is specified by an instruction, the four bits contained in the specified index register are ORed with the low-order four bits of a "root" address to generate a 12-bit address. Only the low-order eight bits of that address are utilized when a data memory address is formed.

The controller instruction set contains twenty-one data-memory reference instructions, thirteen X-register only instructions, three types of (conditional) branch instructions and eighteen miscellaneous instructions; a total of fifty-five instructions. An assembler has been developed which permits control programs to be written in mnemonic form; it is described in Appendix I. Input and output instructions are provided which permit direct addressing of sixteen input and output devices, respectively. Tri-state devices are employed to instrument the (sixteen-bit) input bus. At room temperature, the controller is capable of operating at a cycle time of approximately 180 nsec.; the machine is actually operated at a rather conservative cycle time of 235 nsec. The relatively high operating speed has been achieved by over-lapping the addressing phase of an instruction's execution with the execution phase of the preceding instruction, and by extensive utilization of Shottky TTL devices to instrument the controller.

To maintain circuit complexity at a reasonable level, the controller hardware was designed to service a single interrupt signal. A low to high transition of that signal causes execution of the (background) control program to be interrupted if the interrupt mode of operation has been enabled by the control software. On servicing an interrupt, the address of the next instruction to be executed in the background program is stored in location 0 of the data memory, the program counter is set to zero, and the interrupt mode of operation is disabled. Normally, the instructions contained in the first few locations of the control memory will cause execution of an interrupt service routine if an appropriate flag has been set by the software. Requiring a flag to be set before branching to the interrupt service routine permits an initialization subroutine to be executed before entering the interrupt routine. The interrupt mode of operation is normally reenabled by an appropriate instruction immediately before returning to the background program.

Four subsystems within the modem and the external computer at a network control terminal interact with the controller on an interrupt basis. Interrupts generated by any of these are accommodated through the use of peripheral hardware and software. Each subsystem which interacts with the controller on an interrupt basis initiates an interrupt request by causing an interrupt

flip-flop contained within the subsystem to be set. The interrupt flip-flop outputs are ORed to generate the controller interrupt signal and are made available to the controller input bus as an interrupt identification word. The interrupt routine or routines which should be executed in response to an active controller interrupt signal are identified by the interrupt service routine. This is accomplished by inputting the interrupt identification word to the X-register via an input instruction and then determining which bit or bits in that word are set. Each interrupt routine contains an output instruction which, on execution, causes the associated interrupt flip-flop to be cleared.

3. The Slot Timing and Control Subsystem

The slot timing and control subsystem (see Figure 3) contains two circuits which interact with the digital controller on an interrupt basis: a receive slot rollover circuit and a transmit slot rollover circuit. Those circuits generate pulsed waveforms in synchronism with a receive clock and a transmit clock, respectively, which have periods equal to the slot duration. The beginning of a slot in the receive time base, is marked by the occurrence of a pulse in the receive slot rollover waveform. Each pulse in that waveform causes a receive slot interrupt flip-flop to be set which, in turn, causes execution of a receive slot interrupt routine by the digital controller. A software counter is maintained by that routine which designates the location of the current slot relative to the beginning of the signaling frame, i.e., the slots are organized into subframes and the subframes into frames by the system software. Each time the receive slot interrupt routine is executed, the software slot counter is incremented, all processing operations to be performed during the following slot are identified, and execution of those operations is initiated. The latter function is accomplished by outputting a receive control word to a receive control buffer contained within the slot timing and control subsystem. On the occurrence of a pulse in the receive slot rollover waveform, i.e., at the beginning of the following slot, the contents of the receive control buffer are transferred to a receive control latch. In turn, the latch outputs either activate or inhibit operation of the various receive circuits during the slot, depending on the structure of the receive control word. Control over circuits contained in the transmit subsystem is accomplished in the same manner, i.e., a transmit slot interrupt routine operates in conjunction with a transmit control buffer and a transmit control latch to control the transmit circuits.

All waveforms required to control intraslot operation of the transmit and receive circuits are generated within the slot timing and control subsystem by decoding the outputs of a transmit binary counter (clock) and a receive binary counter (clock), respectively. Each of those counters is cleared (set to zero) by the associated rollover waveform. Thus, all intraslot control waveforms have periods equal to one slot duration. The waveforms employed to toggle the transmit and receive clocks are generated by two nearly-identical time base control counters from a common, fixed-frequency signal. The latter signal is synthesized within the frequency

synthesis and control sybsystem from the output of a 1 MHz oven-stabilized crystal oscillator contained within the modem. The use of an external 1 MHz frequency standard can be accommodated by removing a jumper cable on the back panel of the modem and applying the externally-generated signal to the appropriate jack. Each time base control counter contains a controlled-modulus counter followed by a fixed-modulus counter. The controlled-modulus counters provide the mechanism whereby control is exercised over the transmit and receive time bases. When neither time base is being shifted (corrected), those counters operate modulo-three. To advance the receive time base, the controlled-modulus receive counter is caused to operate modulo-two over an appropriate interval; the time base is retarded by changing the modulus to four. A timing shift equal to one forty-eighth of a code symbol duration ($\Delta/48$ sec.) is introduced each time the time base correction circuit undergoes a full cycle of operation. Thus a $\pm \Delta/96$ sec. quantization error is associated with the correction mechanism. Control over the number of operating cycles completed by the two time base correction circuits each time a correction is enabled is provided by a down-counter and associated mode control circuits. To enable a correction, a time base control word is output from the digital controller to a time base control circuit. Twelve bits of that word convey the number of $\Delta/48$ sec. increments contained in the correction to be made; those bits are loaded into the down counter. Two bits in the control word designate the correction mode and one bit designates the sign of the timing correction; these latter bits are stored in a control latch. The latch outputs cause appropriate gates to be enabled during the correction interval. A transition of the down-counter outputs to a *nonzero* state is sensed by circuits which respond to enable a correction cycle and toggle the down-counter in sequence until the counter returns to the zero state. If the X-STRAP (cross strap) switch (see Figure 1) is in the up position and the appropriate mode control bit is set, the transmit and receive time bases are shifted by equal amounts but in opposite senses. This feature is used to provide doppler compensation to the transmit time base on an open-loop basis.

The amount by which the transmit time base is advanced relative to the receive time base can be both monitored and set under program control. At the beginning of each slot in the receive time base, the contents of the (binary) transmit clock are stored in a latch; the latch outputs are made available to the controller input bus. Thus, a measure of the timing differential (modulo one slot duration) can be made available to the software by executing an appropriately-addressed input instruction. To set relative timing, a circuit which inhibits toggling of the transmit clock is activated under program control and the desired relative time displacement is the output to the transmit clock. Reactivation of the toggle input to the transmit clock occurs automatically at the beginning of the following receive slot. Initiation of the read and set operations at instants in time which result in proper circuit operation is assured by incorporating the instructions which cause those operations to be performed in the receive slot interrupt routine.

4. The Correlation Processor

The time base correction circuits, the digital controller, and the correlation processor (see Figure 3) jointly form two sampled-data delay lock loops. One loop provides closed-loop control over the receive time base and, if desired, open-loop control over the transmit time base; the other loop controls the transmit time base on a closed-loop basis. Normally, the correlation processor is operated sequentially to process the network clock pulses received during the network clock slots and the R portions of the received L/R bursts during the assigned R slots (in the receive time base). The mode in which the correlation processor operates during each slot in the receive time base is determined by the states of selected receive control latch outputs and, thus, by the digital controller. Two reference signals are generated within that processor which have essentially the same temporal structure during a slot as the signal being processed during that slot. The reference signals differ in that the codes employed to generate them are displaced in time by Δ seconds; the timing of one code (or pair of codes) is advanced by $\Delta/2$ seconds relative to the receive clock and the other code (or pair of codes) is retarded in time by $\Delta/2$ seconds relative to the receive clock. Both the "early" and "late" codes (or code pairs) are impressed as biphase (or quadraphase) modulation on a doppler-corrected local oscillator (LO) signal to generate the reference signals; the frequency of the LO signal is nominally equal to 59.3 MHz. The received (70 MHz) signal is multiplied by each of the correlation processor reference signals in separate IF-correlator channels. Estimates of the cross correlations between the modulations contained on the received signal and on the reference signals are obtained by bandpass filtering the lower sideband components of the input by reference signal products -- the 10.7 MHz components -- and "linearly" detecting the filter outputs. The two detector outputs are added and subsequently sampled at appropriate instants in time to provide a sampled sum output; similarly, the outputs are subtracted and sampled to provide a sampled-difference output. The sampled-sum and sampled-difference outputs are both proportional to the level of the signal processed during the slot when the received signals's time base is displaced relative to the receive clock by no more than $\Delta/2$ seconds. The sampled-difference output is also proportional to the time base displacement provided the magnitude of that displacement doesn't exceed $\Delta/2$ seconds.

A twelve bit analog to digital (A/D) converter is employed sequentially to convert the sampled (and held) outputs of the correlation processor into digital representations. A correlation processor interrupt flip-flop is set following completion of each A/D conversion. On servicing a correlation processor interrupt request, the digital controller executes a correlation processor interrupt routine. That routine, in part, performs processing operations on the digital data generated by the A/D converter, enables execution of background routines, as approrpriate, and causes the correlation processor interrupt flip-flop to be cleared. When the timing loops are operating in a closed-loop mode, the background

routines calculate timing corrections from the converted-sum and converted-difference data and output the corrections in an appropriate form to the time base control circuit. The calculations performed on the sum and difference data obtained through processing of the network clock pulses include the addition of four sum and four difference samples obtained in the succession,* division of the accumulated data by the accumulated sum data when the accumulated sum exceeds a "breakpoint,"** and multiplication of the normalized difference data (error estimate) by an appropriate constant to form the correction. The normalization operation maintains the receive-loop gain at approximately one independent of the signal level when the breakpoint data constant is exceeded by the accumulated sum. No data averaging is performed in calculating a (closed-loop) transmit time base correction; otherwise, the calculations performed in estimating the timing errors within the two loops are similar.

5. Delay Lock Loop Control Concept

A delay-lock loop does not respond to make the timing error small if the magnitude of the error is greater than $3\Delta/2$ seconds; thus, means must be provided for acquiring timing initially through open-loop control, enabling closed-loop operation, identifying loss of lock, and reacquiring proper timing after loss of lock has been identified. In the TDMA modems, all acquisition, reacquisition, and status identification operations required to instrument the two sampled-data delay lock loops are performed under software control by the digital controller. Consequently, the sophisticated operations and decision mechanisms needed to achieve a high level of design effectiveness are easily provided. No attempt will be made here to document the acquisition/reacquisition algorithms in detail. Rather, procedures for enabling acquisition and simplified descriptions of the techniques employed to acquire proper timing relationships will be presented. The documentation of the software employed is contained in Appendix I.

6. Receive Time Base Acquisition Procedures and Techniques

Following initialization of controller operation, acquisition of proper receiver timing is enabled automatically if the REACQ/PAUSE switch (see Figure 1) is in the REACQ position. During acquisition of the receive time base, the receive clock is advanced in one-Δ increments until the total timing shift equals one slot duration (146Δ), the maximum timing uncertainty of the modulo one-slot receive (hardware) clock.

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*The number of data samples accumulated is determined by a software data constant; thus, that number can easily be changed.

**Otherwise, the accumulated difference is divided by the breakpoint data constant.

The transmit/receive code generators are set to initial states at the beginning of each transmit/receive slot. Thus, although the codes employed repeat after 127 symbols, the effective code period equals 146Δ. Following each timing shift, the correlation processor is enabled to operate during each of thirty-two successive slots with the early and late codes (or code pairs) which have the same structure as the code (or code pair) contained on the network clock signal applied to that processor's reference inputs. Each of the resulting thirty-two sampled-sum outputs generated by the correlation processor is read by the digital controller and compared with the largest preceding output. If an output exceeds the largest preceding output, the latter output is set equal to the current sum output, an overshift variable is set to zero, and the value of the receive-slot software counter during which the response occured is stored in an appropriate location of the data memory. Should all thirty-two samples be smaller than the largest preceding output, the overshift variable is (effectively) incremented by Δ seconds. The procedure is repeated if a threshold level defined by the software is not exceeded by the largest response observed and if the REACQ/PAUSE switch was not placed in the PAUSE position during the search cycle. If the threshold is exceeded, the receive time base is corrected for the overshift introduced following occurrence of the largest sampled-sum output, the receive slot counter is set to zero at an appropriate time as determined from the stored value of that counter, and a lock validation phase of operation is enabled. A search for the clock pulses which occupy two consecutive slots at the beginning of each frame, i.e., subframe identification (see Figure 2), is initiated following a valid lock indication. Successful completion of the receive time base acquisition algorithm results in the SRCH and NO LOCK CLK lamps (see Figure 1) being extinguished.

7. Transmit Time Base Acquisition Procedures and Techniques

Two means are provided for establishing proper transmitter timing at a terminal when the modem is configured to establish the LRF. If the terminal/satellite round-trip propagation delay is not known a priori to within plus or minus one-half of the slot duration -- approximately ± 400 μsec -- initial transmitter timing is established by the coarse range subsystem (see Figure 3) operating in conjunction with the digital controller. When enabled, the coarse range subsystem causes the transmission of a low-level, pulsed-envelope, frequency-swept signal. The amplitudes of the normal and coarse-ranging signals can both be adjusted from the front panel. The center frequency of the "coarse-ranging" signal is near the first null in the spectra of all other signals employed. Signal transmission is enabled for one complete subframe per signaling frame in synchronism with the transmit clock. The subframe occupied by each transmitted pulse is calculated from the modem's address and remains fixed from frame to frame.*

*The coarse range address is not unique since only sixteen addresses are available for use by the forty-four terminals which can be accommodated by the overhead allocation.

A digital frequency-synthesis circuit is enabled each time that subframe occurs which causes the signal frequency to be swept over approximately 10 KHz in a nominally-linear fashion during the pulse on time. The transmitted coarse ranging signal is subsequently received on the down-link and processed by a coarse range processor. That processor essentially estimates the cross correlation between the frequency-sweep modulations contained on the received coarse ranging signal and on a reference signal which is generated in synchronism with the receive clock. The reference signal is frequency-swept in exactly the same manner as the transmit signal, but during the assigned subframe of the receive clock, and is employed as the LO input to one of four down-converters contained within the coarse range processor. When the time base of the received coarse-ranging signal coincides with the receive time base, the desired signal at the output of the third down-converter has a constant frequency of 40 KHz during the assigned subframe (provided the system frequency uncertainties equal zero). The noise bandwidth at the third down converter's output is nominally equal to 20 KHz. The desired correlation estimate is obtained by amplitude limiting the 40 KHz signal, down-converting the limited signal to 10 KHz, bandpass filtering the 10 KHz signal to a noise bandwidth of approximately 150 Hz, envelope detecting the filter output signal, and low-pass filtering the detector output. A threshold detector is employed to compare the output of the low-pass filter with a manually-set threshold voltage. That detector's output is made available to the digital controller input bus.

Acquisition of transmitter timing to within the accuracy required to transmit a pulse which arrives at the satellite within the assigned L/R slots, i.e., coarse range acquisition, is performed under program control. Following depression of the CRS RNG ACQ momentary switch (see Figure 1), the CRS RNG ACQ lamp is caused to blink and the transmit time base is set in advance of the receive time base by an integer number of slot durations.* That number can equal either of two data constants defined by the software depending on the position of the DLY SEL switch. The data constants have been assigned values which are appropriate when the modem is operated in conjunction with a satellite at a near-synchronous altitude. When the terminal is closer to the suborbital point of the satellite than to the satellite horizon, the DEL SEL switch should be placed in the D1 position; otherwise, the D2 position is applicable. If the modem is operated in conjunction with a terrestrial relay or a satellite in a nonsynchronous orbit, utilization of the coarse range subsystem requires changing the software data constants corresponding to switch positions D1 and D2 to appropriate values; the contents of an arbitrary data memory location can be changed via the six character octal switch register and the LD ADR and LD MEM momentary switches (see Figure 1).

*The operations described are inhibited (delayed) if the receive timing loop is not operating in the closed-loop mode.

After the transmit time base has been set, transmission of the coarse ranging signal is enabled and the output of the threshold detector in the coarse range processor is input to the controller near the end of the subframe assigned for coarse range acquisition as determined from the receive (software) clock. The transmit time base is delayed by one-sixth of a slot duration following processing of each coarse range pulse until either a threshold crossing has been identified and validated or a search limit imposed by the software is attained. A validated threshold crossing results in the CRS RNG ACQ lamp being extinguished and enabling of a fine range acquisition mode. The latter operation causes the FN RNG ACQ lamp to blink. If a validated threshold crossing does not occur before search is terminated, the CRS RNG ACQ lamp is turned on continuously.

During fine range acquisition, i.e., during acquisition of precise transmitter timing, a pulse having a one-slot duration is transmitted within each L/R slot pair assigned to the modem (as determined from the transmit clock). The leading edge of each fine range acquisition pulse occurs near the center of the corresponding L slot. The correlation processor is operated in a fine range acquire mode during each occurrence of the L/R overhead slots as determined from the receive clock. Proper transmitter timing is identified by comparing the sampled-sum output of the correlation processor following processing of the fine range acquisition pulse with a threshold equal to one-half of the average value of four successive sampled-sum outputs resulting from network clock pulse processing. The transmit time base is successively advanced and delayed in a pattern which provides the equivalent of a one-Δ search increment until an acquisition criterion is satisfied or a search limit imposed by the soft-ware is attained. If the acquisition criterion is satisfied, the FN RNG ACQ and NO LOCK RNG lamps are turned off, the TX RDY lamp is lit, and a closed-loop mode of operation is enabled. Otherwise, the FN RNG ACQ lamp is lit continuously.

The fine range acquisition mode of operation can also be enabled by depressing the FN RNG ACQ momentary switch.* On responding to the switch closure, the control program causes the FN RNG ACQ lamp to blink, sets the transmit clock relative to the receive clock, and enables the fine range search procedure. Again, the amount by which the transmit clock is initially advanced relative to the receive clock equals either of two values depending on the position of the DEL SEL switch. When that switch is in the D1 position, the initial offsets set into the hardware and software transmit counters are taken from two data memory locations which are loaded from the front panel. In utilizing this

*The coarse range subsystem is inoperative when the modem is configured to establish the HRF; thus, for that configuration, the fine range acquisition mode is the only means available for establishing proper transmitter timing.

mode of operation, the integer number of data slot durations contained in the available terminal/satellite round-trip propagation delay estimate is loaded into one data memory location and a representation of the residual fractional-slot duration contained in the estimate is loaded into a second location before depressing the FN RNG ACQ momentary switch. Alternatively, a previously-measured value of the round trip delay which is stored in two other data memory locations can be employed to set the transmit counters by placing the DEL SEL switch in the d2 position. This latter procedure should be employed only if the two timing loops were operating closed-loop in the recent past.

8. The Differential Detector

The differential detector generates a baseband representation of the data contained on signals received during selected time slots. Operation of the differential detector is inhibited when the receive timing loop is considered "out of lock" by the control software. Both the transmit and receive timing loops must be considered locked before the transmission of pulses during data slots is enabled. Two down conversions are performed within the differential detector. The LO signal employed in the first down conversion is generated by biphase/quadraphase modulating a doppler-corrected 59.3 MHz sinusoid with an "in-phase" code/code pair. Multiplying that LO signal with the received signal and bandpass filtering the 10.7 MHz component of the multiplier output results in removal of the spectrum-spreading code and compensation of the down-link doppler. A 10.7 MHz variable-gain amplifier and associated control circuits are employed to provide automatic gain control (AGC) on an open-loop basis. An estimate of the network clock signal amplitude is employed to control the amplifier gain. That estimate is generated by sampling and holding the correlation processor sum output at appropriate instants in time, and lowpass filtering the output of the sample/hold circuit. The amplitude-controlled 10.7 MHz signal is multiplied by two phase-quadrature 10.7 MHz LO signals in separate mixers. Each mixer is followed by a baseband amplifier, an integrate/dump circuit, and a sample/hold circuit. The outputs of the two sample/hold circuits can be considered as the orthogonal components of a vector which respresents the received signal during the interval (data bit) in which they were generated. The sampled and held values of the integrator outputs are applied sequentially to an 8-bit A/D converter by an analog multiplexer. Digital representations of the signal "vector" generated by the A/D converter are subsequently processed by digital circuits which form the dot product of successive vectors. When that product is positive or zero, the detector outputs a zero; otherwise, the detector outputs a one. Subsequent processing and/or management of the detected data is performed either by the I/O device buffers as described previously or by the link buffer, depending on the slot in which the data is received.

9. The Link Buffer

The link buffer (see Figure 3) interfaces the linking and network control algorithms with the receive and transmit subsystems. Data received serially during all L/R slot pairs and during selected LLL NCT overhead slots (see Figure 2) is formatted into successive bytes containing eight bits each by the receive portion of the link buffer. A link interrupt flip-flop is set after each complete byte has been received. On servicing a link interrupt, the digital controller reads the buffer contents, performs intermediate processing operations, sets flags to enable background routines, as appropriate, and clears the link interrupt flip-flop. All linking and network control words transmitted in the L/R and LLL assignments are converted from an asynchronous parallel format to a synchronous serial format by the transmit portion of the link buffer. The entire word to be transmitted is output to the buffer during the slot immediately preceding the overhead assignment in which transmission is to occur on execution of an output instruction contained in the transmit slot interrupt routine. Accommodation of the twenty-four bit network control words is achieved by allocating two device addresses to the buffer. The low order sixteen bits of each network control word are output to one address and the high order eight bits are output to another address on execution of separate output instructions. Note that the address of a network control terminal must be selected so that the LLL and L/R assignments are not contiguous if the buffer is to operate properly. The transmit slot interrupt routine also contains instructions which cause an appropriate transmit control word to be output to the transmit control buffer. As described previously, the control word is loaded into a transmit control latch at the beginning of the following slot. Serial transmission of the control word from the buffer is enabled when selected outputs of the transmit control latch are active.

10. The Frequency Synthesis and Control Subsystem

Efficient operation of the differential detector and the correlation processor requires that the center frequencies of the second IF signals differ from 10.7 MHz by no more than approximately 200 Hz and 1.6 KHz when the LRF and HRF are established, respectively. An automatic frequency control (AFC) loop maintains the frequency offsets resulting from relative satellite/terminal (aircraft) motion at acceptable values when the modem is operated in conjunction with a UHF satellite and in the LRF mode.* A 10.7 MHz voltage controlled oscillator (VCO) provides

*Doppler tracking would not be required if the HRF could be employed in conjunction with a UHF satellite; however, the UHF channels currently available do not have bandwidths adequate for supporting the HRF. If a SHF satellite is employed, control over the frequencies of the LO signals used to down-convert the received signal to 70 MHz and up-convert the 70 MHz transmit signal to the transmit band must be provided by an external subsystem, e.g., a beacon track subsystem. Alternatively, means for performing a two-dimensional frequency/time search could be incorporated within the modem.

the variable frequency capability required to instrument that loop. Signals synthesized from the VCO signal include the nominal 59.3 MHz first LO signal and a 70 MHz signal which is modulated to generate the IF transmit signal. Generation of the 59.3 MHz LO signal is accomplished by mixing the VCO output signal with a fixed-frequency 70 MHz signal and bandpass filtering the lower sideband component of the product signal. The nominal 80.7 MHz upper-sideband component is mixed with a fixed-frequency 10.7 MHz signal to generate the nominal 70 MHz signal. The fixed-frequency 10.7 MHz and 70 MHz signals are synthesized from the 1 MHz reference oscillator signal within the frequency synthesis and control subsystem. If the VCO signal frequency equals 10.7 MHz + Δf and the frequency errors associated with the fixed-frequency signals are assumed to equal zero, then the synthesized signals have frequencies of 59.3 MHz - Δf and 70 MHz + Δf. Thus, if the frequency error in the received signal is due solely to down-link doppler and the VCO loop operates to maintain the second IF at exactly 10.7 MHz, then the down-link doppler will be impressed open-loop on the transmit frequency in an inverted sense. This approach to doppler compensation is imperfect since the signals actually transmitted to and received from the satellite have different carrier frequencies; thus, those signals experience different doppler shifts. While the design is adequate for current UHF applications, a significant improvement in other frequency bands can be achieved by replacing the analog VCO with two digital frequency synthesizers which have digital control inputs. Accurate control over both the transmit and receive frequencies can then be provided by the digital controller. This alternative approach may be incorporated in later models.

The AFC loop operates to maintain the difference between the crossover frequency of a 10.7 MHz frequency discriminator and the frequency of the down-converted network clock signal at a small value. An estimate of that difference is obtained by summing the two 10.7 MHz correlation processor IF signals, soft limiting the sum signal, processing the soft limited signal with the frequency discriminator, and sampling the discriminator output at appropriate instants. The sampled values are filtered (integrated) to generate the VCO control voltage. Control over the mode in which the AFC loop operates is provided by the digital controller. In addition to the closed-loop mode of operation, the VCO control voltage can be held at a current value or set to zero. The latter mode is enabled during acquisition of the receive clock since a signal appropriate for extracting an error estimate is not available when the receiver is improperly timed. An initial network clock signal frequency offset up to approximately 500 Hz or 4 KHz can be tolerated during acquisition of receiver timing depending on whether the LRF or HRF is established, respectively. After proper receiver timing has been established, the closed loop and hold operating modes are enabled, as appropriate, depending on the state of the receive timing loop. A control override switch which is accessible from the front panel can be activated to prevent the AFC loop from being enabled.

11. The 75 bps Buffer

The 75 bps buffer is designed to operate in conjunction with a serial I/O teleprinter which contains TTL-compatible I/O circuits. The symbols applied to the buffer input must have a nominal duration of 1/75 second. The transmit portion of the buffer can be used either to accept data from the teleprinter for immediate transmission or to store messages composed off-line for subsequent transmission; stored messages can contain up to sixty-four characters. A universal, asynchronous receiver/transmitter (UAR/T) device contained within the buffer functions, in part, to identify and discard the start and stop bits associated with each character output by the teleprinter. Eight symbols, e.g., a seven-bit ASCII character and an associated parity bit, are buffered and subsequently transmitted at the burst rate for each character input to the modem. Data received in bursts on the down-link during time slots in which the teleprinter is operating is processed by the receive portion of the 75 bps buffer. Circuits within the buffer cause the received data to be discarded until two carriage return characters are detected in succession. Normally, data received after consecutive carriage returns have been detected is output to the teleprinter if (and only if) the SEND/RCV switch is in the RCV position. The teleprinter can be operated in an echo mode, however, by setting a mode switch accessible from the front panel to the appropriate position. Of course, this mode of operation is useful only when the data bit length associated with the teleprinter assignment is compatible with the terminal's receive capabilities. The receive portion of the buffer is disabled on detection of two consecutive control D characters, or on a transition of the SEND/RCV switch from SEND to RCV. Data stored in both the transmit and receive portions of the buffer is cleared out on a SEND to RCV transition.

12. The 2400 bps Buffer

The 2400 bps buffer provides a plus/minus six volt military standard interface between the modem and a 2400 bps I/O device. Data input to the buffer must be generated in synchronism with a (continuous) 2400 Hz transmit clock provided by the modem. The input symbols are stored temporarily and output from the buffer at the instantaneous data rate during the assigned data slots. Normally, data is extracted from the buffer at an average rate exactly equal to the rate at which it is filled. Data received in bursts during appropriate slots is input to the receive portion of the buffer. Subsequently, the data is output to the external device at a uniform 2400 bps rate in synchronism with a 2400 Hz receive clock if a data transfer criterion is satisfied. The transfer of data is inhibited when the external send/receive switch is in the send position and the DPLX/SMPLX switch is in the SMPLX position (see Figure 1). If a simplex assignment is in use, an echo mode of operation can be established by placing the DPLX/SMPLX switch in the DPLX position after the assignment has been established. Start and stop bits are appended to each received character by the UAR/T before the character is output to the teleprinter.

SECTION IV
OPERATING PROCEDURES

1. Introduction

Operating procedures are described in this section which apply when the modem has been properly aligned, and calibrated, and when all test mode and configuration (behind the panel) switches are in the proper position (Table III). The procedures given through Section 8 apply at all terminals in the network. At network control terminals, which use random-access memories, additional operating procedures must be followed as described in Appendix III.

Immediately before the modem is turned on, the transmit network clock switch must be off at terminals not assigned to transmit the network clock signal; all other front-panel toggle switches can be positioned arbitrarily at those terminals when power is applied. At the terminal assigned to transmit the network clock signal, the network clock is on, the switch inhibit ranging loop corrections switch is in normal position, and the inhibit transmitter switch in in normal position. These latter switch positions may be established either before or after the modem is turned on.

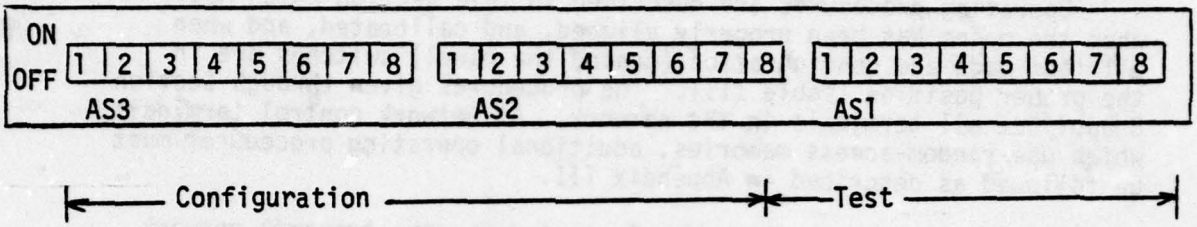
2. Power Turn-On and Turn-Off

Power is applied to the modem by depressing the standby power switch and then the operate switch. Depressing the standby switch applies power to the 1 MHz reference oscillator and the 10.7 MHz VCXO. From a cold start, these oscillators should be turned on for approximately thirty minutes to allow stabilization of their frequencies before operating the modem. To turn the modem off completely, the operate switch should be depressed before pressing the standby switch. It is recommended that standby power be applied continuously when possible.

3. Operating the Clock Loop

The receiver gain should be set approximately half-scale on the noise level meter when receive noise is present in the system. Automatic acquisition of the network clock is enabled by depressing the master clear momentary switch with the reacquisition-pause toggle switch in the acquisition position. The search light will flash until the initial acquisition algorithm has progressed to the point where shifting the time base in one chip increments is no longer required at which time the search light is extinguished. The no-lock clock light is extinguished after the initial acquisition algorithm has been completed successfully. Should a valid lock fail to be established or the receiver lose the network clock, automatic reacquisition will occur unless the reacquisition-pause switch is placed in the pause

TABLE III
Configuration and Test Switches



	Configuration Switches		
Switch	Function		
AS3-1	MSB	Modem Address	OFF=1 ON =0
AS3-2			
AS3-3			
AS3-4			
AS3-5			0,1, and 4n where n=1,2,... are disallowed (base ten) addresses. For low rate format, AS3-1, AS3-2, and AS3-3 are on.
AS3-6			
AS3-7			
AS3-8			
AS2-1	LSB		
AS2-2	NCT		OFF at network control terminal
AS2-3	MSB	NCTADR	Network control terminal address
AS2-4	LSB		00 is disallowed
AS2-5	HRF		OFF for high rate format
AS2-6	2ϕ/4ϕ		OFF for biphase - ON for quadraphase
AS2-7	CRTTY		ON for TTY echo

Test Switches

AS2-8	INRCM	OFF inhibits receive code modulation	norm. ON
AS1-1	CPEN	ON enables correlation processor continuously	norm. OFF
AS1-2	DDEN	ON enables differential detector continuously	norm. OFF
AS1-3	AFCINH	OFF inhibits AFC	norm. ON
AS1-4	CONTX	ON enables continuous transmission	norm. OFF
AS1-5	NOCODM	OFF inhibits normal code modulation	norm. ON
AS1-6	DATMINH	OFF inhibits data modulation	norm. ON
AS1-7	UMLLTX	OFF enables unmodulated low-level transmission	norm. ON
AS1-8	UMTX	ON inhibits transmitter phase modulation	norm. OFF

position. After the network clock signal has been acquired the receiver gain can be readjusted so that location 000256$_8$ on the octal display reads approximately 002000$_8$. (See Table IV for information contained in memory and corresponding memory locations.)

4. Operating the Range-Tracking Loop

To acquire proper transmitter timing at terminals not transmitting the network clock signal, inhibit range switch and inhibit transmitter switch must both be in the normal position, and the network clock loop locked. The cross strap switch may be either off or on; its position can be changed at any time. When operating in the low-rate format (LRF) if only a course estimate of the terminal round trip propagation is available *a priori* at the time range loop acquisition is initiated, the delay select switch is set at either the D_1 or D_2 position. If the delay select switch is set at D_2 the range starts at 540$_8$ slots (.293 sec.) and decreases to 448$_8$ slots (.240 sec). In the D_1 position the range starts at 500$_8$ slots (.266 sec) and decreases to 400$_8$ slots (.213 sec.). To initiate coarse range acquisition the coarse range acquisition momentary switch is depressed. This enables a sequence of actions which result in the transmitter being timed to within sufficient accuracy to allow ranging pulses to be transmitted in the periodically occurring link/range slot pairs without overlapping adjacent assignments. The coarse range acquisition light is extinguished on completion of the coarse range acquire algorithm and a fine range acquire algorithm is enabled automatically. When the transmitter timing error has been made sufficiently small, the fine range acquisition light is extinguished and the range tracking loop is enabled. After a valid range loop lock criterion is satisfied, the no-lock range light is extinguished and the transmit ready light is lit. If the acquisition attempt fails at any point in the algorithm, the ranging loop is returned to the pre-initiate-acquisition status and no further action is taken until the coarse range acquisition switch is again depressed. In the event that the valid lock criterion fails to be satisfied after acquisition has been completed, closed-loop corrections to the ranging loop are inhibited and the no-lock range light is lit. Should the valid ranging loop lock criterion again be satisfied within four frames after the no-lock light is lit, the ranging loop is re-enabled and the no lock range light extinguished. Otherwise, a reacquisition algorithm is enabled which causes the transmit time base to be searched over a plus-two-chip to minus-two-chip range. During this time, both the fine range acquisition and the no-lock range lights are lit and the transmit ready light is extinguished. A successful reacquisition attempt results in the fine range acquisition and no-lock range lights being extinguished in that order and the transmit ready light lit. The coarse range acquisition time can be a maximum of 2.75 minutes.

The coarse range acquisition procedure may be by-passed if 1) the round trip delay is known a priori to sufficient accuracy (one half slot ~400 μsec.) when acquisition of transmitter timing is initiated, or 2) a sufficiently short interval of time has elapsed since the two timing loops were properly locked to allow use of the round-trip delay estimate stored in the modem's memory, provided the master clear switch has not been deprssed since the last operation. When the latter case applies, the delay select switch is set to D_2 position and the fine range acquisition switch depressed. This causes the transmitter timing to be advanced relative to the receive clock by an amount equal to the stored round-trip delay estimate and enabling of the fine range acquire algorithm. When a sufficiently accurate round trip delay estimate is available prior to initial locking of the range loop, the coarse range procedure can be bypassed by converting the round trip delay into an octal representation using the procedure given in Appendix IV. The octal representation in terms of slots is loaded into locations 60_8 (coarse range) and the fine range is loaded into location 61_8. The delay select switch is placed in D_1 position and depressing the fine range acquisition switch causes the modem to assume a correct slot count from location 60_8 and proceed to fine range acquisition using the approximate information stored in location 61_8. The coarse range slot count can be displayed by selecting location 210_8 and the fine range count by selecting location 211_8.

Closed-loop corrections to the transmit time base and enabling of the range loop reacquire algorithm can be prevented from occuring by turning the inhibit range switch to inhibit. The transmission of all pulses can then be inhibited by turning the inhibit transmit switch to inhibit. Under these conditions, when the cross-strap switch is on, the transmit timing error will accumulate at a rate determined primarily by the stability of the 1 MHz frequency standard relative to the stability of the network clock signal at the satellite*. If the transmitter and ranging loop are re-enabled (in that order) before the transmitter timing error accumulates to approximately one chip, the ranging loop will lock without enabling of the reaquisition algorithm.

*Up-link doppler experienced by the network clock signal is automatically compensated if the cross strap is enabled at the terminal which transmits the network clock signal.

5. Operating the Switch Register and Display

An octal switch register and octal display are provided on the left side of the control panel to allow displaying and/or altering the contents of selected locations in the random access memory (RAM). The display is enabled by turning display switch to "on". To display the contents of a location in RAM, the location is set into the switch register and the contents are automatically displayed.

The contents of a location in the RAM can be altered by 1) setting the memory location into the switch register, 2) depressing the load address switch, 3) setting the contents to be loaded into the location addressed, and 4) depressing the load memory switch. This feature allows several constants which affect the modem's performance to be altered. Constants loaded from the front panel are returned to their original values when the modem is turned off and back on or when the master clear switch is depressed. A listing of the most useful information contained in memory and the corresponding memory locations is given in Table IV.

6. Procedure for Establishing a Time-Ordered Channel Allocation for Teletype and/or Vocoder

Two means are provided for establishing an assignment of slots in the signaling format under operator control for use in conjunction with a particular I/O device. Normally, assignments would be made by up to three network control terminals on receipt of requests for assignments from the user terminals. To request a data slot assignment one of two request-priority levels and the type of assignment desired are first selected by positioning the appropriate toggle switches on the device control panel. For teletype operation, the bit length switch is set to either short or long bit length (for low-rate format operation only), the priority switch is set to low or high priority, and the send/receive switch to send. For vocoder operation the priority switch is set to high or low priority, the duplex/simplex switch to duplex or simplex, the transmit bit length to short or long bit length (low-rate format only), and the receive bit length to short or long bit length (low rate format only). The request is then initiated by depressing the request assignment switch. The switch closure causes an appropriately-coded sixteen bit control word to be transmitted three times by the modem in its L/R (overhead) assignment; one sixteen bit word is transmitted in each L/R slot pair. Two bits in the control word desginate the particular NCT with which the modem is to interact; those bits are preassigned. The modem at each NCT detects all control words conveyed in the L/R slot pairs and outputs them to an external instrumentation computer. In turn, the control words are processed by a network control algorithm.*

*A network control algorithm has been developed for RADC by the Computer Science Corporation.

A control word is considered valid at a NCT if it has been received in at least two out of three successive L/R assignments of a given terminal and contains NCT identification bits which match that control terminal's address. On receipt of a valid data-slot assignment-request control word, the network control algorithm determines if the request can and should be honored based on the availability of non-assigned time slots capable of supporting the requested data rate and the request priority. If a time ordered channel is to be allocated, two sixteen-bit words are output to the NCT modem; only twenty-four of the thirty-two bits convey control information. The network control words contain, in part, the address of the terminal to which the message is destined as determined by the location of the L/R slot pair in which the assignment request was received, and the identity of the channel being assigned. In turn, the control word is transmitted once in each of three successive LLL overhead slots assigned to the NCT (see Figure 2). Each modem detects all network control words transmitted by the NCT to which it is assigned. Again, at least two out of three successive control words must be identical on detection for the control information to be considered valid. Control word validation is performed in this instance by a digital controller contained within the modem; external computers are required only at the NCT's. A means for loading the control program into the modem is required, however, if volatile random access memory devices are employed to instrument the control memory (Appendix III). The receipt of a validated assignment network control word which contains the modem's address causes the NO ASGN lamp (see Figure 1) to be extinguished and immediate enabling of the assignment if the device is not "busy" servicing a call originated by another terminal. Otherwise, enabling of the assignment is delayed.

A time-ordered channel can also be selected manually by setting an appropriate code word into the octal switches on the device control panel and then depressing the local control switch. A list of allowable teleprinter and vocoder assignments is given in Table V.

7. Linking Procedures - Teletype and/or Vocoder

After a data slot assignment has been received from a network control terminal or manually selected, links with terminals to which information is to be conveyed can be established. To link with a particular terminal, the address of that terminal (located on the configuration and test switch panel - Table II) and a number designating the destination device (1_8 for teletype, 2_8 for vocoder) are set into octal switches on the device control panel, and the REQ LINK momentary switch is depressed. This causes two sixteen-bit link control words to be formulated by the modem's digital controller. The first word conveys the destination-terminal/device-number address and control bits for distinguishing the link request from other types of control words; the second word contains, in part, the data slot assignment on which the link is to operate. Each word is transmitted three times in a total of six successive L/R slot pairs assigned to the modem at which the link

request is initiated. All control words conveyed in the L/R slot pairs are detected at each modem. When a link-request control word is received at a modem which contains the modem's address, a link validation algorithm is initiated by the modem's digital controller. First, the L/R slot pair in which the provisional link request was received, i.e., the calling terminal's address, and the control word are saved in memory. Two control words are subsequently detected during the following two L/R slot pairs which have addresses matching the stored address.* If at least two of the three detected control words are identical and the matching words are appropriately coded, the digital controller performs a similar two-out-of-three test on control words detected during the four following occurrences of the appropriate L/R slot pair. The operations following receipt of a validated "second" word depend on the status of the device being called. If the device is not busy and the send/receive switch is in the receive position,** operation of the device on the assignment conveyed by the validated second word is enabled, the NO LINK lamp on the control panel is extinguished, and an "acknowledge-proceed" control word containing the address of the calling terminal is transmitted three times by the called terminal in the L/R slot pair assigned to the latter terminal. On receipt of a validated acknowledge-proceed control word at the calling terminal in the L/R assignment of the terminal being called, the NO LINK lamp is extinguished. If the device called is busy or the SEND/RCV switch is in the SEND position, and if the received link request has not been preceded by a request having the same or higher priority as the current request, an acknowledge-busy control word containing the calling terminal's address is transmitted three times, appropriate information is stored in a call-waiting table, and the CALL WTNG lamp is either lit continuously or caused to blink. A blinking CALL WTNG lamp indicates that the received link request has been assigned a high priority by the calling terminal. Reception of a validated acknowledge-busy code word at the calling terminal causes the NO LINK and RDY lamps to be extinguished. Should a high priority link request be received at a terminal after receipt of a waiting, low-priority call and before the latter call has been serviced, the low-priority call is "bumped" by successively transmitting three terminate-link control words containing the low-priority caller's address and three acknowledge-busy control words containing the address of the high priority caller in the L/R overhead assignment.*** Also,

*Each slot address occurs once per frame.

**A send/receive switch is not provided on the 2400 bps device control panel; it has been presumed that an appropriate switch will be available as an integral part of the I/O device.

***In concept, an arbitrary number of waiting calls could be maintained in a queue. The data and control memories within the prototype modems are not sufficiently large to store and service more than one waiting call at a time.

the CALL WTNG lamp is caused to blink. The receipt of a validated terminate-link control word at a calling terminal after receipt of a validated acknowledge-busy control word causes initialization of the control routine (software) and the control panel lamps to the state that existed before the link was requested.

An established link can be terminated at either the called or calling device by depressing the CLR momentary switch. This causes the transmission of three terminate-link control words which contain the address of the terminal with which the device is linked. When a link is terminated either under local control or on receipt of a validated terminate-link control word, a check is made to determine if a call is waiting. If a call is waiting and the SEND/RCV switch is in the RCV position, the following operations are performed: 1) information contained in the call-waiting table is transferred to a busy table, 2) operation of the I/O device is enabled on the time-ordered channel indicated by the "second" link request control word received previously, 3) the CALL WTNG, NO LINK, and RDY lamps are extinguished if necessary, and 4) an acknowledge-proceed control word containing the address of the calling terminal is transmitted three times in the appropriate L/R assignment. The servicing of a waiting call is inhibited (delayed) if the SEND/RCV switch is in the SEND position. If a call is not waiting following termination of a link or if the SEND/RCV switch is in the SEND position, operation of the device on its assignment is enabled if the device has an assignment;* otherwise, the device is disabled.

8. Procedures for Terminating an Allocation

An assignment is relinquished irrespective of the manner in which it was obtained by depressing the REL ASGN momentary switch; the switch closure is disregarded if the assignment is in use. The NO ASSN lamp is lit immediately when the assignment is relinquished. Should that lamp not come on, depressing the CLR and REL ASGN momentary switches in succession will cause the channel to be released. If the assignment was received from a NCT, depressing the REL ASGN momentary switch causes an assignment-relinquished network control word to be transmitted three times (provided the switch closure is not disregarded). The detection of a validated assignment-relinquished network control work at a NCT causes the status of the relinquished time slots to be changed from "in use" to "available for assignment".

The LLL overhead slots allocated to a NCT can be used to request the relinquishment of an assignment made by that control terminal if appropriate provisions are incorporated in the network control algorithm. The modem is currently configured so that the receipt of a validated relinquish-assignment network control causes a REL ASGN lamp to blink; depression of the REL ASGN momentary switch is required before the assignment is actually relinquished.

*An assignment can be used to establish links in sequence after a link request has been received from another terminal if the SEND/RCV switch is in the SEND position each time a link is terminated.

TABLE IV
DATA MEMORY LOCATION AND CONTENTS

Location	Symbol	Description
0040	MRSYNC	Receive Sync Mask
0041	RSYNCT	Receive Sync Time
0042	MTSYNC	Transmit Sync Mask
0043	TSYNC	Transmit Sync Time
0050	RORNG	Rollover Value of Range Counter, LRF
0051	RORNGH	Rollover Value of Range Counter
0056	RTSD1	Number of Slots in Initial Round Trip Delay for D1 Position
0057	RTSD2	Number of Slots in Initial Round Trip Delay for D2 Position
0060	IRNG1	Number of Slots Contained in RTD when FNRNG Enabled Using the D1 Position
0061	IRNG2	Initial Value of Range Counter when FNRNG is Enabled Using the D1 Position
0062	SCHINC	Search Increment 48 $\approx$ One Chip (Δ)
0063	DCNTMX	Maximum Value of a Clock Loop Acquisition Counter
0064	CLAQTH	Clock Loop Acquisition Threshold
0065	CLSCMX	Maximum Value of a Clock Loop Search Counter
0066	CLPCMX	Maximum Value of a Clock Loop Pulse Counter
0071	AVNUM	Number of Clock Pulses Processed to Obtain One Clock Loop Error Estimate
0075	CLTHMN	Minimum Value of Accumulated Sum Signal for Clock Loop Track to be Maintained
0076	SFCTMX	Maximum Number of Subframes Contained in the Double-Pulse Search Interval
0077	LOFCMX	Maximum Number of Subframes Missed Before Loss of Clock Loop Lock is Declared
0102	RAQCMX	Maximum Value of a Range Loop Acquisition Counter
0103	RLSCMX	Maximum Value of a Range Loop Search Counter
0104	RLPCMX	Maximum Value of a Range Loop Pause Counter
0113	CRSINC	Coarse Range Search Increment '102200 $\sim$ One Sixth of One Slot
0114	CRSCMX	Maximum Value of a Coarse Range Search Counter
0115	CRPCMX	Maximum Value of a Coarse Range Pause Counter
0117	CRDLY	Maximum Number of Slots Contained in the Clock Loop Acquisition Interval if Coarse Ranging is to Proceed Automatically
0120	FRDLY	Maximum Number of Slots Contained in the Clock Loop Acquisition Interval if Fine Ranging is to Proceed Automatically

TABLE IV (Cont)

0121	RLDLY	Maximum Number of Slots Contained in the Clock Loop Acquisition Interval if Fine Ranging is to be Enabled Automatically
0210	RANGE1	Number of Slots Contained in the Round Trip Delay when Course Ranging Has Been Acquired
0211	RANGE2	Value of the Range Counter When Fine Ranging has Been Acquired
0256	SCCSUM	Sampled Clock Count Sum an Indicator of the Received Clock Signal Level
0257	RSUM	The Value of the Course Range Search Counter an Indicator of the Received Range Pulse Level

TABLE V
Allowable Assignments

Format	Rate	SF nr	Slot nr
HRF	75	- -($\overline{0\ 0\ 0\ 0\ 0}$)	0 0 0 0 1
		- - X X X X X	($\overline{0\ 0}$)X X X
	2400	- - - - - - - -	($\overline{0\ 0}$)X X X
LRF LBL	75	- -($\overline{0\ 0}$)	0 0 0 0 1
		- - X X	($\overline{0\ 0}$)X X X
	2400	- - - -	($\overline{0\ 0}$)- - -
LRF SBL	75	X X($\overline{0\ 0}$)	0 0 0 0 1 X
		X X X X	($\overline{0\ 0}$)X X X X
	2400	- - - -	($\overline{0\ 0}$)X X X -

Only time slots greater than 7 are allowed because the network control overhead occupies most of the first 8 slots. Digits like $\overline{00}$ or $\overline{00000}$ indicate that 00 or 00000 may not be used for these digits.

APPENDIX I
TDMA MODEM CONTROLLER

I. GENERAL

A. CONTROL MEMORY: 2048 16-bit words
(expandable to 4096)

B. DATA MEMORY: 256 16-bit words

C. REGISTERS:

1. X Register: 16-bit accumulator
2. C Register: 1-bit carry register
3. I, J, K Registers: 4-bit index registers
4. PC Register: 12-bit program counter

D. ADDRESS FORMATION

Instruction addresses in the control memory are taken from the Program Counter which normally advances one address for each instruction executed. The Program Counter is loaded with new addresses by branch instructions and by interrupts. When a short branch instruction is executed, the last eight bits of the instruction word are concatenated with the high order four bits of the Program Counter, forming a 12-bit address. If the instruction specifies indexing, the four bits of the specified Index Register are ORed with the low order four bits of the 12-bit address.

Long branch instructions consist of two words. The address is taken from the low order twelve bits of the second word. If indexing is specified, the index bits are ORed. When an interrupt occurs the Program Counter is loaded with 0.

Data memory addresses are taken from the low order eight bits of data memory reference instructions. If the instruction specifies indexing, the contents of the specified Index Register are ORed with the low order four bits of the address.

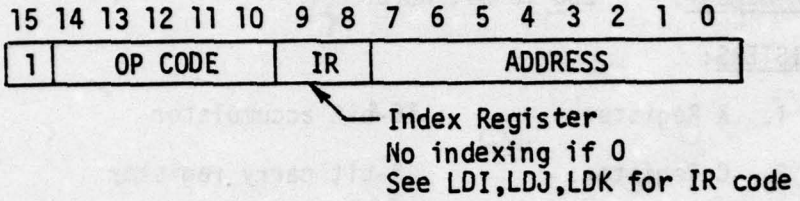
E. INTERRUPTS

One interrupt is provided. If the interrupt is enabled by an IEN instruction and the interrupt line is true, an interrupt will occur at the end of the current instruction. The computer will save the address of the next instruction to be executed in location 0 of the Data Memory and branch to location 0 of the Control Memory. The interrupt will be automatically disabled until reenabled by an IEN instruction. The interrupt process takes one cycle. When the IEN, BRS, CMP, TDM, or TST instructions are executed, interrupts are delayed until the following instruction is executed.

II. INSTRUCTIONS

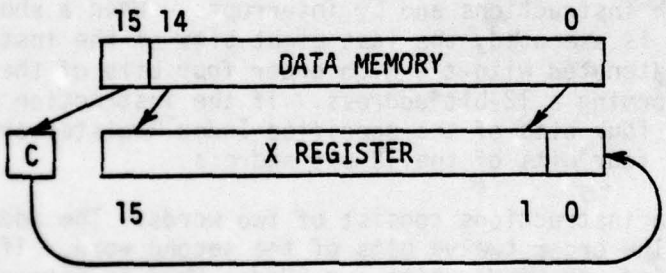
A. DATA MEMORY REFERENCE INSTRUCTIONS

1. Format:



2. Example:

INST.	OP CODE	FUNCTION	TIME(cycles)
LDL	00000	Load X Left Shifted	1



$DM_{0-14} \rightarrow X_{1-15}$

$DM_{15} \rightarrow C$

$C \rightarrow X_0$

3. Instructions

INST.	OP CODE	FUNCTION	TIME(cycles)
LDL	00000	Load X Left Shifted $DM_{0-14} \longrightarrow X_{1-15}$ $DM_{15} \longrightarrow C$ $C \longrightarrow X_0$	1
LDR	00001	Load X Right Shifted $DM_{1-15} \longrightarrow X_{0-14}$ $DM_0 \longrightarrow C$ $C \longrightarrow X_{15}$	1
LDC	00010	Load X Complemented $\overline{DM_{0-15}} \longrightarrow X_{0-15}$	1
LDX	00011	Load X $DM_{0-15} \longrightarrow X_{0-15}$	1
LDD	01110	Load X Indirect Thru Data Memory $DM_{0-15} \longrightarrow X_{0-15}$ The contents of bits 0-7 of the data memory address specified in the operand subfield are taken as a data memory address. X_{0-15} is loaded from this address.	2

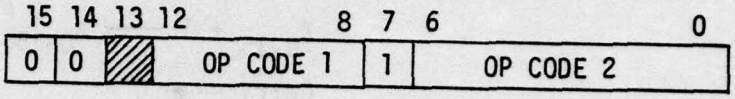
INST.	OP CODE	FUNCTION	TIME(cycles)
ADD	00100	Add to X $DM_{0-15} + X_{0-15} \longrightarrow X_{0-15}$ Carry $\longrightarrow$ C	1
SUB	00101	Subtract from X $X_{0-15} - DM_{0-15} \longrightarrow X_{0-15}$ Borrow $\longrightarrow$ C	1
CMP	11000	Compare Same as SUB but the X Register and C Register are not changed. A branch instruction should follow immediately. One instruction must be completed after CMP before interrupt can occur.	1
TDM	11100	Test Data Memory Condition (positive, negative, zero, etc.) of DM_{0-15} is tested. A branch instruction should follow immediately. One instruction must be completed after TDM before interrupt can occur.	1
AND	00110	AND to X DM_{0-15} AND $X_{0-15} \longrightarrow X_{0-15}$	1

INST.	OP CODE	FUNCTION	TIME(cycles)
TST	11001	Test Same as AND but X and C Registers are not changed. A branch instruction should follow immediately. One instruction must be completed after TST before interrupt can occur.	1
OR	00111	OR to X DM_{0-15} OR $X_{0-15} \longrightarrow X_{0-15}$	1
XOR	01000	Exclusive OR to X $DM_{0-15} \oplus X_{0-15} \longrightarrow X_{0-15}$	1
ADC	01001	Add with carry to X $DM_{0-15} + X_{0-15} + C \longrightarrow X_{0-15}$ Carry $\longrightarrow$ C	1
SBC	01010	Subtract with carry from X $X_{0-15} - DM_{0-15} - C \longrightarrow X_{0-15}$ Borrow $\longrightarrow$ C	1
MPS	01011	Multiply Step If C = 0 $DM_{1-15} \longrightarrow X_{0-14}$ $0 \longrightarrow X_{15}$ $DM_0 \longrightarrow C$	1

INST.	OP CODE	FUNCTION	TIME(cycles)
MPS (Cont'd)		If C = 1	
		$DM_{0-15} + X_{0-15} \rightarrow X_{0-14}$	
		$0 \rightarrow X_{15}$	
		$DM_0 + X_0 \rightarrow C$	
DVS	01100	Divide Step	1
		If X < DM	
		Borrow → C (zero for + numbers)	
		If X ≥ DM	
		$X_{0-15} - DM_{0-15} \rightarrow X_{0-15}$	
		Borrow → C (1 for + numbers)	
STZ	11010	Store Zero	1
		$0 \rightarrow DM_{0-15}$	
STO	11011	Store Ones	1
		$177777_8 \rightarrow DM_{0-15}$	
STX	01101	Store X	1
		$X_{0-15} \rightarrow DM_{0-15}$	
STD	01111	Store X indirect thru Data Memory	2
		$X_{0-15} \rightarrow DM_{0-15}$	
		The contents of bits 0-7 of the data memory address specified in the operand subfield are taken as a data memory address. X_{0-15} is stored into this address.	

B. X REGISTER ONLY INSTRUCTIONS TIME - 1 cycle

1. Format



Bits shown shaded in all formats are assigned zeroes by the assembler.

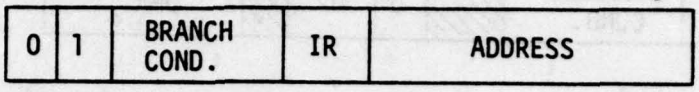
2. Instructions:

INST.	CODE	FUNCTION
LS	017677	Left Shift X $X_{15} \rightarrow C$ $X_{0-14} \rightarrow X_{1-15}$ $0 \rightarrow X_0$
LSC	013677	Left Shift X and C $X_{15} \rightarrow C$ $X_{0-14} \rightarrow X_{1-15}$ $C \rightarrow X_0$
RS	017737	Right Shift X $X_0 \rightarrow C$ $X_{1-15} \rightarrow X_{0-14}$ $0 \rightarrow X_{15}$
RSC	013737	Right Shift X and C $X_0 \rightarrow C$ $X_{1-15} \rightarrow X_{0-14}$ $C \rightarrow X_{15}$

INST.	OP CODE	FUNCTION
INC	011740	Increment X $X_{0-15} + 1 \longrightarrow X_{0-15}$ Carry $\longrightarrow$ C
DEC	017757	Decrement X $X_{0-15} - 1 \longrightarrow X_{0-15}$ Borrow $\longrightarrow$ C
SOC	010600	Set to One C $1 \longrightarrow$ C
CLC	016600	Clear C $0 \longrightarrow$ C
CMC	014600	Complement C $\overline{C} \longrightarrow$ C
SOX	001774	Set to Ones X $-1 \longrightarrow X_{0-15}$
CLX	001763	Clear X $0 \longrightarrow X_{0-15}$
CMX	001760	Complement X $\overline{X_{0-15}} \longrightarrow X_{0-15}$
NOP	000200	No Operation

C. SHORT BRANCH INSTRUCTIONS

1. Format:



2. Instructions:

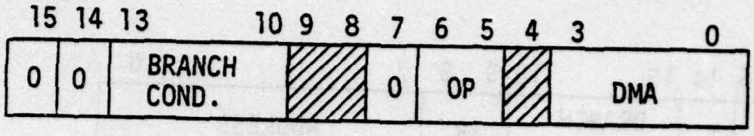
INST.	FUNCTION	TIME(cycles)
BR	Short Branch If the BRANCH COND. is satisfied, the address formed from PC_{8-11}, ADDRESS and the Index Register, if specified, is loaded into the Program Counter. See LDI,LDJ, LDK for IR code.	1

BRANCH COND.		BIT 13	12	11	10
Carry	(C)	0	1	0	0
No Carry	(NC)	1	1	0	0
X = 0	(EQ)	0	1	1	1
X < 0	(LT)	0	0	0	1
X $\leq$ 0	(LE)	0	0	1	1
Uncond. Branch		1	1	0	1
X $\neq$ 0	(NE)	1	1	1	1
X $\geq$ 0	(GE)	1	0	0	1
X > 0	(GT)	1	0	1	1

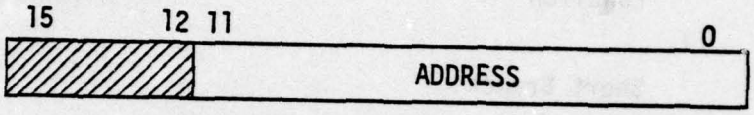
D. LONG BRANCH INSTRUCTIONS

1. Format:

WORD 1



WORD 2



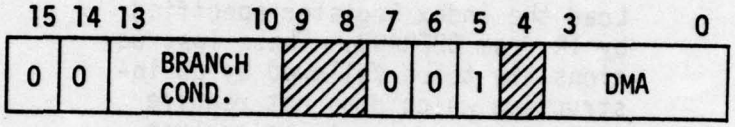
2. Instructions:

INST.	OP CODE	FUNCTION	TIME(cycles)
BRL	10	Branch Long If BRANCH COND. is satisfied (see short branch instruction), the 12 bits of ADDRESS are loaded into the Program Counter.	2
BRS	11	Branch to Subroutine Same as BRL except that the Program Counter is stored at the data memory location specified by DMA ($0\text{-}17_8$). Storing occurs regardless of whether or not a branch occurs. One instruction must be completed after BRS before interrupt can occur.	3

E. MISCELLANEOUS INSTRUCTIONS

INST.	FUNCTION	TIME(cycles)
SRT	Subroutine Return	2 if branch occurs 1 if no branch occurs

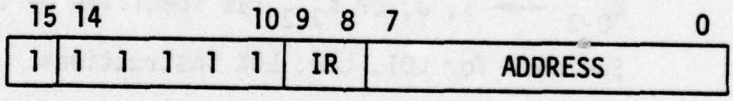
Format:



The contents of the data memory location specified by DMA are loaded into the Program Counter if the BRANCH COND. is satisfied.

BRI,BRJ,BRK	Decrement Index and Branch	1

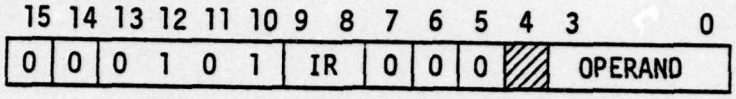
Format:



Register I, J, or K as specified by IR is decremented. If the result is 17_8, no branch occurs. The Program Counter is loaded with the address formed by the four high order bits of the Program Counter and the eight bits of ADDRESS if the result is not 17_8. See LDI,LDJ,LDK for IR code.

INST.	FUNCTION	TIME(cycles)
LDI,LDJ,LDK	Load Index Immediate	1

Format:

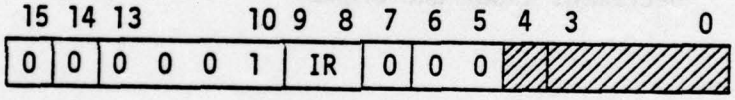


IR	REG.
00	None
01	I
10	J
11	K

Load the Index Register specified by IR from OPERAND. These instructions are to be followed by an instruction which does not require an indexed address to be generated or a NOP instruction.

TXI,TXJ,TXK	Transfer X to Index	1

Format:

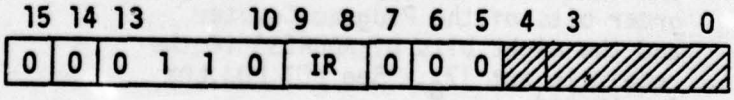


$X_{0-3} \longrightarrow$ I, J, or K_{0-3} (as specified by IR)

See note for LDI, LDJ, LDK instructions.

TIX,TJX,TKX	Transfer Index to X	2

Format:



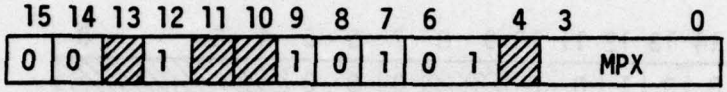
I, J, or $K_{0-3} \longrightarrow X_{0-3}$ (as specified by IR)

$0 \longrightarrow X_{4-15}$

See LDI, LDJ, LDK for IR code.

INST.	OP CODE	FUNCTION	TIME(cycles)
INP	011240	Input	1

Format:



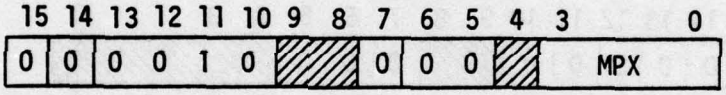
INPUT BUS ⟶ X_{0-15}

$\overline{\text{INPUT FLAG}}$ ⟶ C

MPX ⟶ MULTIPLEXER

OUT — Output — 3

Format:

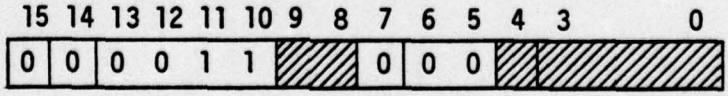


MPX ⟶ MULTIPLEXER

Contents of X Register are placed on Output Bus. Strobe is sent during the second cycle of the instruction.

IEN — Interrupt Enable — 1

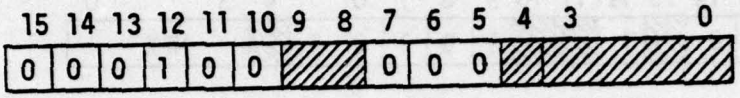
Format:



One instruction must be completed after IEN instruction before interrupt can occur.

INST.	FUNCTION	TIME(cycles)
IDS	Interrupt Disable	1

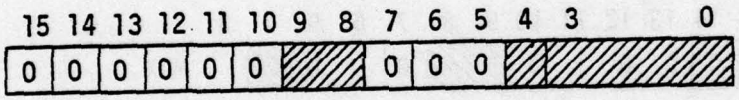
Format:



The interrupt is disabled immediately on execution of IDS instruction.

HLT — Halt Computer

Format:



Computer executes the next instruction after the halt and then stops.

III. ASSEMBLER

An assembler statement is made up of four fields: the label field, the operation field, the operand field and the comment field. Not all fields are necessarily used in a given instruction. The fields are separated by one or more spaces.

A. LABEL FIELD:

The label field always starts in column 1. If a label is not used, column 1 should be blank. Labels consist of from one to six ASCII characters other than "+", "-","*", ",". The first character must be alphabetic.

B. OPERATION FIELD:

The operation field consists of one of the computer instruction mnemonics or a pseudo OP mnemonic. Pseudo OPs are:

EQU	- Equivalence
ORG	- Sets the Origin
DATA	- Generates constants
BS	- Assigns one or more memory locations for storage.

C. OPERAND FIELD:

The operand field consists of one or more subfields, separated by commas, which specify symbolic addresses, indexing, etc.

D. COMMENT FIELD:

The comment field is last in the line and may contain any text. An asterisk in column 1 makes the entire line a comment.

E. EXPRESSIONS:

Expressions consist of numbers and symbols (from label fields) which may be added or subtracted.

*	=	"THIS LOCATION"
20	=	20_{10} DECIMAL
'20	=	20_{8} OCTAL
"101	=	5_{10} BINARY

D. EXAMPLES OF ASSEMBLER STATEMENTS

LABEL	OPERATION	ADDRESS,INDEX	COMMENT
Data Memory Reference Instruction			
DNEG	LDX	ABC+2,J	LOAD FROM TABLE
X-Register Instruction			
QUOT	INC		INCREMENT X
			No operand field; comment follows operation.
Short Branch Instruction*			
RPOS	BRGE	XYZ+2,K	
Long Branch Instruction*			
LOC5	BRPGE	XYZ+2	
			Generates two words; address goes into second word.
Subroutine Call Instruction*			
	BRSGE	XYZ+2,10	
			The number 10 designates the data memory location in which the return address is stored.
Subroutine Return Instruction*			
	SRTGE	10	
			The number 10 designates the data memory location from which the return address is taken.

LABEL	OPERATION	ADDRESS,INDEX	COMMENT

BRI,BRJ,BRK Instructions

	BRI	XYZ+2

Load Index Immediate Instruction

	LDI	3

TXI,TXJ,TXK,TIX,TJX,TKX,IEN,IDS,HLT Instructions

	TXI	

No operand field required. All after operation field is considered comments.

INP,OUT Instructions

	INP	A/D

A/D is defined by an equivalence statement, e.g., A/D EQU 6.

*The last two letters of the BR, BRP, BRS, and SRT instructions represent the Branch Condition (see P. 40). An unconditional branch will occur if there is no suffix.

IV. ADDITIONAL NOTES ON SOFTWARE

If the index registers are loaded by use of the TXI,TXJ, TXK,LDI,LDJ, or LDK instructions, the actual loading takes place during the execution of the next instruction. As a result, if the instruction immediately following one of these six instructions specifies indexing, the instruction will be indexed by the previous contents of the Index Register. For example, assume that Index Register I has 7_8 as its contents prior to encountering the following instructions:

```
.
.
.
LDI    3
STX    LOC,I
.
.
.
```

This sequence of instructions will result in storing the contents of the X Register in (LOC)V(7) rather than (LOC)V(3). Note that the result (LOC)V(3) will result if an instruction is inserted between the LDI and STX instructions

Branch instructions are used to alter the contents of the Program Counter. Short branches can be used to branch to locations within page boundaries of the Control Memory. Each page in the Control Memory is 256 locations in length. Long branches must be used for crossing page boundaries.

In using the BRS instruction, the location for storing the address of the next instruction must be specified as an octal number from 0_8 to 15_8. Normally, locations 0_8 to 15_8 of the Data Memory are reserved exclusively for storing return addresses. Note that when BRS instructions are nested, each instruction must specify a different storage location for the next instruction. Similar precautions must be observed when a subroutine is called in an interrupt service routine (e.g., an interrupt occurs when the main program is in a subroutine).

APPENDIX II
CONTROL MEMORY CONTENTS

The following listing consists of two parts. The first is a variable table which first lists all the variable names appearing in Data Memory and their locations. Then, a list of all the variable names appearing in the control memory program along with their locations follows immediately. The second part is an assembly language description of both Data Memory and Control Memory contents. It will be noted that the first 126_8 locations of data memory are designated by the pseudo mnemonics DAT and EQU. These locations are used for constants or variables which must be initiated. The values associated with each are actually contained in the first 126_8 locations of control memory so that they may be restored when MSTR. CLR. is depressed. The rest are designated by either BS or EQU. These locations contain variables which do not require initialization. This allows the origin of the program to be placed at location 127_8 of control memory without affecting the program operation when MSTR/CLR is depressed.

	SYMBOL	LOCATION
3		
4	ZERO	0000
5	FMT	0004
6	M'17	0005
7	M'177	0006
8	M'1777	0007
9	M'3	0010
10	M'37	0011
11	MSUBFR	0011
12	MDEVSW	0011
13	PCNTMX	0011
14	M'377	0012
15	MBYTE	0012
16	M'3777	0013
17	M'7	0014
18	M'77	0015
19	M'777	0016
20	MLPSW	0016
21	M'7777	0017
22	M'30	0020
23	M'300	0021
24	M'60	0022
25	M'600	0023
26	MASG	0023
27	M'6000	0024
28	M'7000	0025
29	M'160	0026
30	MDEV	0026
31	M'360	0027
32	C'17	0030
33	C'3777	0031
34	C17777	0032
35	C37777	0033
36	M'1700	0034
37	D24	0035
38	MDSPLY	0036
39	DSPLYT	0037
40	MRSYNC	0040
41	RSYNCT	0041
42	MTSYNC	0042
43	TSYNCT	0043
44	MFMT	0044
45	MTADR	0045
46	MNCTID	0046
47	MRANGE	0047
48	RORNG	0050
49	RORNGH	0051
50	SOFCW	0052
51	CSOCW	0053
52	S/DMOD	0054
53	LNKRCW	0055
54	RTSD1	0056
55	RTSD2	0057
56	IRNG1	0060
57	IRNG2	0061
58	SCHINC	0062
59	DCNTMX	0063
60	CLAQTH	0064
61	CLSCMX	0065
62	CLPCMX	0066
63	VCLCMX	0067
64	CLTCMN	0070
65	AVNUM	0071
66	CLATM	0072
67	DECAYM	0073
68	THINCM	0074
69	CLTHMN	0075
70	SFCTMX	0076
71	LOFCMX	0077
72	SDPATM	0100
73	SDPVTM	0101
74	RAQCMX	0102
75	RLSCMX	0103
76	RLPCMX	0104
77	VRLCMX	0105
78	RLTCMN	0106
79	SRLTHM	0107
80	BSADR1	0110
81	BSADR2	0111
82	JMPINC	0112
83	CRSINC	0113
84	CRSCMX	0114
85	CRPCMX	0115
86	CRTCMN	0116
87	CRDLY	0117
88	FRDLY	0120
89	RLDLY	0121
90	CLGF	0122
91	RLGF	0123
92	SCGCBP	0124
93	RGCBP	0125
94	BSADR3	0126
95	SINTWD	0127
96	XSTORF	0130
97	CSTORE	0131
98	MEMADR	0132
99	CRADR	0133
100	LRADR	0134
101	NCTSLT	0135
102	NCTID	0136
103	TADR	0137
104	MBIT0	0140
105	MBIT1	0141
106	MBIT2	0142
107	MBIT3	0143
108	MBIT4	0144
109	MBIT5	0145
110	MBIT6	0146

111	MBIT7	0147
112	MBIT8	0150
113	MBIT9	0151
114	MBIT10	0152
115	MBIT11	0153
116	MBIT12	0154
117	MBIT13	0155
118	MBIT14	0156
119	MBIT15	0157
120	TEMP	0160
121	DMADR	0160
122	TEMP1	0161
123	PROD	0161
124	DMADMX	0161
125	TEMP2	0162
126	MCNC	0162
127	DEN	0162
128	TEMP3	0163
129	MPLR	0163
130	NUM	0163
131	OLAMPS	0164
132	LAMPS	0166
133	TEMP4	0167
134	SIGN	0167
135	SWFLGS	0170
136	TEMP5	0173
137	DSWTCH	0174
138	SWITCH	0176
139	ITEMP	0177
140	DSPADR	0177
141	HORCNT	0200
142	RCNTR	0201
143	RSLOT	0202
144	TCNTR	0203
145	TSLOT	0204
146	ECWD0	0205
147	ECWD1	0206
148	ECKDUF	0207
149	RANGE1	0210
150	RANGE2	0211
151	CTLWTF	0212
152	CTLWCT	0212
153	RCVRPT	0213
154	SRCVCW	0214
155	SCNT	0215
156	RBYTE1	0215
157	SRSLOT	0216
158	RBYTE	0216
159	LKENBL	0217
160	CPENBL	0220
161	OVRINC	0221
162	SWPNTR	0221
163	CLPNTR	0222
164	RNGTYP	0223
165	C/SUMO	0224
166	SOFLG	0225
167	SPSUM	0226
168	FMLKTH	0226
169	DCNTR	0227
170	RBYTNO	0227
171	PCNT	0230
172	LWCNTR	0230
173	CLTRK	0231
174	CLKLPF	0232
175	RNGLPF	0233
176	LINKF	0234
177	CLIMIT	0235
178	RCWMOD	0236
179	CLFLG	0237
180	RCVEN	0240
181	ENRCV	0240
182	RDRNGF	0241
183	DPFLG	0242
184	FRMLK	0243
185	SFCT	0244
186	LOFC	0244
187	NUMAV	0245
188	CCSUM	0246
189	CCDIF	0247
190	CLCORR	0250
191	RLCORR	0251
192	CLPC	0252
193	CLFSCH	0252
194	RLPC	0253
195	RLFSCH	0253
196	CLSC	0254
197	SRCHCT	0254
198	RLSC	0255
199	SCCSUM	0256
200	RSUM	0257
201	CRSC	0257
202	SCCDIF	0260
203	RDIF	0261
204	RLIMIT	0261
205	CLSCHT	0262
206	SRCH	0262
207	RLSCHT	0263
208	RAQC	0264
209	RLAQF	0265
210	TXCLKF	0266
211	TXRPT	0267
212	STXCW	0270
213	TXEN	0271
214	ENTX	0271
215	RLTRK	0272
216	RLFLG	0273
217	TXACWF	0274
218	RPTXED	0275
219	CLTC	0276
220	RLTC	0277

221	CRTC	0277
222	VCLC	0300
223	VRLC	0301
224	CRPC	0301
225	TXLWCT	0302
226	TXLWPT	0303
227	ARLKWD	0304
228	RTNNCT	0306
229	LSADR	0310
230	JMPSGN	0313
231	NRLKWD	0314
232	NCTW1R	0314
233	NCTW2R	0317
234	LRLKWD	0320
235	LCLKWD	0324
236	ORLKWD	0330
237	OCLKWD	0334
238	BADRT	0340
239	WADRT	0342
240	CADRT	0344
241	CPNTR	0346
242	TLKWD1	0350
243	TLKWD2	0352
244	NXTASG	0354
245	ASMT	0356
246	MTX	0360
247	MRCV	0362
248	TXTBL	0364
249	RCVTBL	0366
250	TXCW	0370
251	RCVCW	0372
252	DLYC	0374
253	RLCOR1	0375
254	ENCORR	0376
255	LKWCCT	0127
256	TERMLK	0136
257	LASMT?	0147
258	ENASG?	0155
259	ENLASG	0162
260	TERMEX	0174
261	ENCALL	0176
262	ASSIGN	0221
263	TTY	0227
264	TTYSBL	0237
265	TTYLBL	0247
266	VOC	0251
267	SVSBL	0261
268	SVLBL	0265
269	ASGCON	0266
270	FDVOC	0277
271	FDSBLR	0326
272	FDLBLR	0332
273	FDSBLT	0344
274	FDLBLT	0350
275	FORMCW	0354
276	INTID	0373
277	TSINTR	0403
278	RSINTR	0405
279	LKINTR	0407
280	CPINTR	0412
281	INTRTN	0414
282	LKINT	0420
283	LKINT0	0437
284	LKINT1	0447
285	LKINT2	0466
286	LKIE1	0506
287	CPINT	0513
288	A/DINP	0516
289	CPINT1	0541
290	CPINT2	0550
291	CPINT3	0560
292	CPINT4	0563
293	CRSCOR	0571
294	CPINT5	0601
295	CPINT6	0606
296	INPCS	0614
297	INPCD	0622
298	INPCSO	0630
299	CPINT7	0636
300	INPRS	0642
301	INPRD	0644
302	CPIE	0651
303	RSINT	0655
304	LPLMP	0677
305	DEVLMP	0707
306	SWTCH	0714
307	DSPLY1	0723
308	DSPLY2	0736
309	DSPLY3	0742
310	DSPLY4	0752
311	RSYNC?	0762
312	CLCT1	0777
313	CLCT2	1030
314	CLCT3	1047
315	CLCT4	1064
316	RLCT1	1066
317	RLCT2	1101
318	RLCT3	1104
319	RLCT4	1116
320	RLCT5	1132
321	RLCT6	1141
322	RLCT7	1147
323	RLCT8	1153
324	RLCT9	1157
325	RSLT01	1170
326	RORNG	1206
327	OPTST	1216
328	RSLT02	1231
329	RSLT03	1233
330	RSLT04	1240

331	RSLT05	1245
332	RCVD1	1251
333	LKRNG	1262
334	TSTRP	1301
335	RPCONT	1306
336	NCTTST	1313
337	RSLT0	1323
338	NCT1	1335
339	NCT2	1342
340	NCT3	1344
341	RSIE1	1350
342	RSIE2	1351
343	RSIE3	1352
344	RSIE4	1354
345	STZBS	1361
346	INITTX	1372
347	TXOVHD	1413
348	CLKTST	1424
349	TSTCKF	1427
350	TXCLK	1453
351	SCHREQ	1470
352	TSINT	1474
353	TXCK?	1521
354	TSTCL	1526
355	TSTRL	1530
356	FNRNG	1540
357	CRSRNG	1550
358	TSINT1	1557
359	TSINT2	1574
360	TSLT01	1600
361	TSLT02	1604
362	TSINT3	1606
363	TLNK0	1615
364	TLNK1	1627
365	TLNK2	1650
366	TLNK3	1657
367	TLNK4	1663
368	TSLT11	1667
369	TSLT12	1706
370	TSLT13	1715
371	TSLT0	1717
372	TSIE0	1736
373	TSIE1	1740
374	ECINT	1750
375	ECINT0	1760
376	ECINT1	1765
377	SEARCH	1771
378	CLROUT	2010
379	DBLP0	2033
380	DBLP1	2045
381	DBLP2	2062
382	CLROU1	2071
383	CLROU2	2107
384	CLCOR1	2156
385	CLCOR2	2200
386	CLPAUS	2214
387	CLVER1	2225
388	CLTST1	2242
389	CLTST2	2251
390	CLTST3	2274
391	CLTST4	2277
392	CLSRCH	2312
393	CLABT	2317
394	STRDLY	2332
395	REQSCH	2335
396	CLEXIT	2343
397	MULT	2345
398	CORR	2360
399	TC/SM	2365
400	CORR0	2374
401	CORR1	2401
402	CORR2	2422
403	CORREX	2432
404	RLROUT	2433
405	RLPAS1	2465
406	RLVER1	2472
407	RLTST1	2503
408	RLTST2	2513
409	RLSCH	2527
410	RLSCH1	2562
411	RLABT	2567
412	RLEXIT	2575
413	INITRL	2577
414	RLIN1	2623
415	RLIN2	2644
416	RLIN3	2655
417	RLIN4	2666
418	RLIN5	2673
419	RLIN6	2710
420	RLIN7	2714
421	RLIN8	2717
422	RLINEX	2722
423	INIT	2724
424	LRF	2744
425	HRF	2761
426	INIT1	2775
427	CLRBS	3016
428	RUN	3034
429	INITCL	3036
430	CLRRTN	3051
431	RLRRTN	3054
432	LKRRTN	3057
433	SWROUT	3065
434	SWCONT	3140
435	CLRLNK	3157
436	TSTBMP	3175
437	LOCALL	3206
438	LCLCNT	3213
439	RELASG	3230
440	LCLASG	3250

```
441   NOTLCL      3255
442   RELCOM      3267
443   CLRREL      3276
444   REGASG      3300
445   REGAS1      3324
446   REGLNK      3327
447   SWEXIT      3351
448   TST2/3      3352
449   T2/3EX      3365
450   RSADR       3371
451   LKROUT      3404
452   LINK0       3416
453   LINK1       3470
454   LINK2       3476
455   LINK3       3503
456   LINK4       3507
457   LINK5       3511
458   LINK6       3541
459   LINKEY      3545
460   VCALL?      3547
461   VCALL1      3557
462   VCALL2      3564
463   VCALL3      3577
464   VCALL4      3642
465   VCALL5      3646
466   VCALL6      3657
467   VCALL7      3662
468   VCALL8      3676
469   NCTLNK      3702
470   NCTLK1      3726
471   NCTLK2      3752
472   NCTLK3      3760
473   NCTLK4      3771
474   LXEXIT      3774
475
```

```
LOCATION CONTENTS SYMBOL   OPERATION  ADDRESS          COMMENTS
 476
 477                       *TDMA MODEM CONTROLLER PROGRAM, VERSION ONE
 478   00000     170004    ZERO       TDM              FMT
 479   00001     046373               BRLE             INTID
 480   00002     052100               BRP    (I)       INIT
 481             002724
 482   00004     000001    FMT        DAT              1
 483   00005     000017    M.17       DAT              .17
 484   00006     000177    M.177      DAT              .177
 485   00007     001777    M.1777     DAT              .1777
 486   00010     000003    M.3        DAT              3
 487   00011     000037    M.37       DAT              .37
 488             00011     MSUBFR     EQU              M.37
 489             00011     MDEVSW     EQU              M.37
 490             00011     PCNTMX     EQU              M.37
 491   00012     000377    M.377      DAT              .377
 492             00012     MBYTE      EQU              M.377
 493   00013     003777    M.3777     DAT              .3777
 494   00014     000007    M.7        DAT              7
 495   00015     000077    M.77       DAT              .77
```

```
496  00016  000777  M•777     DAT    •777
497          00016  MLPSW     EQU    M•777
498  00017  007777  M•7777    DAT    •7777
499  00020  000030  M•30      DAT    •30
500  00021  000300  M•300     DAT    •300
501  00022  000060  M•60      DAT    •60
502  00023  000600  M•600     DAT    •600
503          00023  MASG      EQU    M•600
504  00024  006000  M•6000    DAT    •6000
505  00025  007000  M•7000    DAT    •7000
506  00026  000160  M•160     DAT    •160
507          00026  MDEV      EQU    M•160
508  00027  000360  M•360     DAT    •360
509  00030  177760  C•17      DAT    •177760
510  00031  174000  C•3777    DAT    •174000
511  00032  160000  C17777    DAT    •160000
512  00033  140000  C37777    DAT    •140000
513  00034  001700  M•1700    DAT    •1700
514  00035  000030  D24       DAT    24
515  00036  177777  MDSPLY    DAT    •177777
516  00037  000000  DSPLYT    DAT    0
517  00040  177777  MRSYNC    DAT    •177777
518  00041  000000  RSYNCT    DAT    0
519  00042  177777  MTSYNC    DAT    •177777
520  00043  000000  TSYNCT    DAT    0
521  00044  000777  MFMT      DAT    •777
522  00045  017600  MTADR     DAT    •17600
523  00046  000177  MNCTID    DAT    •177
524  00047  017777  MRANGE    DAT    •17777
525  00050  011077  RORNG     DAT    •11077
526  00051  001107  RORNGH    DAT    •1107
527  00052  000002  SOFCW     DAT    2
528  00053  011000  CSOCW     DAT    •11000
529  00054  030000  S/DMOD    DAT    •30000
530  00055  000210  LNKBCW    DAT    •210
531  00056  000500  RTSD1     DAT    •500
532  00057  000540  RTSD2     DAT    •540
533  00060  000000  IRNG1     DAT    0
534  00061  000000  IRNG2     DAT    0
535  00062  000060  SCHINC    DAT    48
536  00063  000222  DCNTMX    DAT    146
537  00064  000300  CLAQTH    DAT    •300
538  00065  000010  CLSCMX    DAT    8
539  00066  000020  CLPCMX    DAT    16
540  00067  000004  VCLCMX    DAT    4
541  00070  000002  CLTCMN    DAT    2
542  00071  000004  AVNUM     DAT    •4
543  00072  140000  CLATM     DAT    •140000
544  00073  040000  DECAYM    DAT    •40000
545  00074  110000  THINCM    DAT    •110000
546  00075  000600  CLTHMN    DAT    •600
547  00076  000010  SFCTMX    DAT    8
548  00077  000004  LOFCMX    DAT    4
549  00100  030000  SDPATM    DAT    •30000
550  00101  024000  SDPVTM    DAT    •24000
```

```
551  00102  000002  RAQCMX  DAT  2
552  00103  000074  RLSCMX  DAT  60
553  00104  000004  RLPCMX  DAT  4
554  00105  000004  VRLCMX  DAT  4
555  00106  000002  RLTCMN  DAT  2
556  00107  020000  SRLTHM  DAT  •20000
557  00110  000162  BSADR1  DAT  •162
558  00111  000217  BSADR2  DAT  •217
559  00112  003740  JMPINC  DAT  2016
560  00113  102200  CRSINC  DAT  •102200
561  00114  000600  CRSCMX  DAT  384
562  00115  000007  CRPCMX  DAT  7
563  00116  000005  CRTCMN  DAT  5
564  00117  011610  CRDLY   DAT  5000
565  00120  002734  FRDLY   DAT  1500
566  00121  005670  RLDLY   DAT  3000
567  00122  000030  CLGF    DAT  24
568  00123  000030  RLGF    DAT  24
569  00124  002000  SCGCBP  DAT  •2000
570  00125  000400  RGCBP   DAT  •400
571  00126  000254  BSADR3  DAT  •254
572  00127  000130  SINTWD  BS   1
573  00130  000131  XSTORE  BS   1
574  00131  000132  CSTORE  BS   1
575  00132  000133  MEMADR  BS   1
576  00133  000134  CRADR   BS   1
577  00134  000135  LRADR   BS   1
578  00135  000136  NCTSLT  BS   1
579  00136  000137  NCTID   BS   1
580  00137  000140  TADR    BS   1
581  00140  000141  MBIT0   BS   1
582  00141  000142  MBIT1   BS   1
583  00142  000143  MBIT2   BS   1
584  00143  000144  MBIT3   BS   1
585  00144  000145  MBIT4   BS   1
586  00145  000146  MBIT5   BS   1
587  00146  000147  MBIT6   BS   1
588  00147  000150  MBIT7   BS   1
589  00150  000151  MBIT8   BS   1
590  00151  000152  MBIT9   BS   1
591  00152  000153  MBIT10  BS   1
592  00153  000154  MBIT11  BS   1
593  00154  000155  MBIT12  BS   1
594  00155  000156  MBIT13  BS   1
595  00156  000157  MBIT14  BS   1
596  00157  000160  MBIT15  BS   1
597  00160  000160  TEMP    BS   1
598         00160  DMADR   EQU  TEMP
599  00161  000161  TEMP1   BS   1
600         00161  PROD    EQU  TEMP1
601         00161  DMADMX  EQU  TEMP1
602  00162  000162  TEMP2   BS   1
603         00162  MCND    EQU  TEMP2
604         00162  DEN     EQU  TEMP2
605  00163  000163  TEMP3   BS   1
```

```
606                 00163   MPLR    EQU     TEMP3
607                 00163   NUM     EQU     TEMP3
608   00164       000166    DLAMPS  BS      4
609                 00166   LAMPS   EQU     DLAMPS+2
610                 00167   TEMP4   EQU     DLAMPS+3
611                 00167   SIGN    EQU     TEMP4
612   00170       000173    SWFLGS  BS      4
613                 00173   TEMP5   EQU     SWFLGS+3
614   00174       000176    DSWTCH  BS      4
615                 00176   SWITCH  EQU     DSWTCH+2
616                 00177   ITEMP   EQU     DSWTCH+3
617                 00177   DSPADR  EQU     ITEMP
618   00200       000201    HORCNT  BS      1
619   00201       000202    RCNTR   BS      1
620   00202       000203    RSLOT   BS      1
621   00203       000204    TCNTR   BS      1
622   00204       000205    TSLOT   BS      1
623   00205       000206    ECWD0   BS      1
624   00206       000207    ECWD1   BS      1
625   00207       000210    ECWD0F  BS      1
626   00210       000211    RANGE1  BS      1
627   00211       000212    RANGE2  BS      1
628   00212       000212    CTLWTF  BS      1
629                 00212   CTLWCT  EQU     CTLWTF
630   00213       000214    RCVRPT  BS      1
631   00214       000215    SRCVCW  BS      1
632   00215       000215    SCNT    BS      1
633                 00215   RBYTE1  EQU     SCNT
634   00216       000216    SRSLOT  BS      1
635                 00216   RBYTE   EQU     SRSLOT
636   00217       000220    LKENBL  BS      1
637   00220       000221    CPENBL  BS      1
638   00221       000221    OVRINC  BS      1
639                 00221   SWPNTR  EQU     OVRINC
640   00222       000223    CLPNTR  BS      1
641   00223       000224    RNGTYP  BS      1
642   00224       000225    C/SUMO  BS      1
643   00225       000226    SOFLG   BS      1
644   00226       000226    SPSUM   BS      1
645                 00226   FNLKTH  EQU     SPSUM
646   00227       000227    DCNTR   BS      1
647                 00227   RBYTNO  EQU     DCNTR
648   00230       000230    PCNT    BS      1
649                 00230   LWCNTR  EQU     PCNT
650   00231       000232    CLTRK   BS      1
651   00232       000233    CLKLPF  BS      1
652   00233       000234    RNGLPF  BS      1
653   00234       000235    LINKF   BS      1
654   00235       000236    CLINIT  BS      1
655   00236       000237    RCWMOD  BS      1
656   00237       000240    CLFLG   BS      1
657   00240       000240    RCVEN   BS      1
658                 00240   ENRCV   EQU     RCVEN
659   00241       000242    RDRNGF  BS      1
660   00242       000243    DPFLG   BS      1
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661  00243   000244  FRMLK    BS      1
662  00244   000244  SFCT     BS      1
663           00244  LOFC     EQU     SFCT
664  00245   000246  NUMAV    BS      1
665  00246   000247  CCSUM    BS      1
666  00247   000250  CCDIF    BS      1
667  00250   000251  CLCORR   BS      1
668  00251   000252  RLCORR   BS      1
669  00252   000252  CLPC     BS      1
670           00252  CLFSCH   EQU     CLPC
671  00253   000253  RLPC     BS      1
672           00253  RLFSCH   EQU     RLPC
673  00254   000254  CLSC     BS      1
674           00254  SRCHCT   EQU     CLSC
675  00255   000256  RLSC     BS      1
676  00256   000257  SCCSUM   BS      1
677  00257   000257  RSUM     BS      1
678           00257  CRSC     EQU     RSUM
679  00260   000261  SCCDIF   BS      1
680  00261   000261  RDIF     BS      1
681           00261  RLINIT   EQU     RDIF
682  00262   000262  CLSCHI   BS      1
683           00262  SRCH     EQU     CLSCHI
684  00263   000264  RLSCHI   BS      1
685  00264   000265  RAQC     BS      1
686  00265   000266  RLAQF    BS      1
687  00266   000267  TXCLKF   BS      1
688  00267   000270  TXRPT    BS      1
689  00270   000271  STXCW    BS      1
690  00271   000271  TXEN     BS      1
691           00271  ENTX     EQU     TXEN
692  00272   000273  RLTRK    BS      1
693  00273   000274  RLFLG    BS      1
694  00274   000275  TXACQF   BS      1
695  00275   000276  RPTXED   BS      1
696  00276   000277  CLTC     BS      1
697  00277   000277  RLTC     BS      1
698           00277  CRTC     EQU     RLTC
699  00300   000301  VCLC     BS      1
700  00301   000301  VRLC     BS      1
701           00301  CRPC     EQU     VRLC
702  00302   000303  TXLWCT   BS      1
703  00303   000304  TXLWPT   BS      1
704  00304   000306  AKLKWD   BS      2
705  00306   000310  RTNNCT   BS      2
706  00310   000313  LSADR    BS      4
707           00313  JMPSGN   EQU     LSADR+3
708  00314   000314  NRLKWD   BS      4
709           00314  NCTW1R   EQU     NRLKWD
710           00317  NCTW2R   EQU     NRLKWD+3
711  00320   000324  LRLKWD   BS      8
712           00324  LCLKWD   EQU     LRLKWD+4
713  00330   000334  ORLKWD   BS      8
714           00334  OCLKWD   EQU     ORLKWD+4
715  00340   000342  BADRT    BS      6
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716                 00342  WADRT    EQU      BADRT+2
717                 00344  CADRT    EQU      BADRT+4
718   00346         000350 CPNTR    BS       2
719   00350         000352 TLKWD1   BS       2
720   00352         000354 TLKWD2   BS       2
721   00354         000356 NXTASG   BS       2
722   00356         000360 ASMT     BS       2
723   00360         000362 MTX      BS       2
724   00362         000364 MRCV     BS       2
725   00364         000366 TXTBL    BS       2
726   00366         000370 RCVTBL   BS       2
727   00370         000372 TXCW     BS       2
728   00372         000374 RCVCW    BS       2
729   00374         000375 DLYC     BS       1
730   00375         000376 RLCOR1   BS       1
731   00376         000377 ENCORR   BS       1
732                 000127         ORG      87
733                                *SUBROUTINES START HERE
734                                *LINK WORD TX COUNT SUBROUTINE
735   00127         004010 LKWDCT   OUT      '10 USE ONLY IN
736   00130         106302         LDX      TXLWCT  INTERRUPT
737   00131         017757         DEC      R       ROUTINE UNLESS
738   00132         062134         BRGE     *+2   INTERRUPTS ARE
739   00133         106141         LDX      MBIT1     DISABLED
740   00134         132302         STX      TXLWCT
741   00135         032041         SRT      1
742                                *TERMINATE LINK SUBROUTINE
743   00136         106574 TERMLK   LDX      DSWTCH,I
744   00137         162155         TST      MBIT13
745   00140         076165         BRNE     ENLASG+3
746   00141         162156         TST      MBIT14
747   00142         016042         SRTEQ    2
748   00143         120156         XOR      MBIT14
749   00144         132574         STX      DSWTCH,I
750   00145         164770         STZ      TXCW,I
751   00146         164772         STZ      RCVCW,I
752   00147         162023 LASMT?   TST      MASG
753   00150         076162         BRNE     ENLASG
754   00151         106564         LDX      DLAMPS,I
755   00152         114021         AND      M'37
756   00153         116020         OR       M'30
757   00154         072173         BR       TERMEX-1
758   00155         132756 ENASG?   STX      ASMT,I
759   00156         104143         LDC      MBIT3
760   00157         114564         AND      DLAMPS,I
761   00160         170740         TDM      BADRT,I
762   00161         076174         BRNE     TERMEX
763   00162         106756 ENLASG   LDX      ASMT,I
764   00163         062143         BRS      ASSIGN,3
765                 000221
766   00165         104155         LDC      MBIT13
767   00166         114574         AND      DSWTCH,I
768   00167         132574         STX      DSWTCH,I
769   00170         106564         LDX      DLAMPS,I
770   00171         114014         AND      M'7
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771   00172   116022                OR          M'60
772   00173   164740                STZ         BADRT,I
773   00174   132564   TERMEX       STX         DLAMPS,I
774   00175   032042                SRT         2
775                    *SUBROUTINE FOR ENABLING AN INCOMING CALL
776   00176   132740   ENCALL       STX         BADRT,I
777   00177   116143                OR          MBIT3
778   00200   132704                STX         AKLKWD,I
779   00201   104145                LDC         MBIT5
780   00202   120157                XOR         MBIT15
781   00203   114574                AND         DSWTCH,I
782   00204   116156                OR          MBIT14
783   00205   132574                STX         DSWTCH,I
784   00206   106140                LDX         MBIT0
785   00207   116143                OR          MBIT3
786   00210   114564                AND         DLAMPS,I
787   00211   132564                STX         DLAMPS,I
788   00212   106754                LDX         NXTASG,I
789   00213   162154                TST         MBIT12
790   00214   056221                BREQ        ASSIGN
791   00215   106564                LDX         DLAMPS,I
792   00216   116145                OR          MBIT5
793   00217   132564                STX         DLAMPS,I
794   00220   106754                LDX         NXTASG,I
795                    *SUBROUTINE FOR ENABLING ASSIGNMENT
796   00221   017737   ASSIGN       RS          R
797   00222   132160                STX         TEMP
798   00223   166161                STO         TEMP1
799   00224   164162                STZ         TEMP2
800   00225   162152                TST         MBIT10
801   00226   056251                BREQ        VOC
802   00227   170004   TTY          TDM         FMT
803   00230   062233                BRGE        *+3
804   00231   106007                LDX         M'1777
805   00232   072266                BR          ASGCON
806   00233   017737                RS          R
807   00234   132160                STX         TEMP
808   00235   162155                TST         MBIT13
809   00236   056247                BREQ        TTYLBL
810   00237   106150   TTYSBL       LDX         MBIT8
811   00240   132162                STX         TEMP2
812   00241   106005                LDX         M'17
813   00242   070244                BRNC        *+2
814   00243   106027                LDX         M'360
815   00244   132161                STX         TEMP1
816   00245   106016                LDX         M'777
817   00246   072266                BR          ASGCON
818   00247   106006   TTYLBL       LDX         M'177
819   00250   072266                BR          ASGCON
820   00251   162153   VOC          TST         MBIT11
821   00252   076277                BRNE        FDVOC
822   00253   170004                TDM         FMT
823   00254   042263                BRLT        SVSBL+2
824   00255   017737                RS          R
825   00256   132160                STX         TEMP
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826  00257  162155          TST     MBIT13
827  00260  056265          BREQ    SVLBL
828  00261  106150  SVSBL   LDX     MBIT8
829  00262  132162          STX     TEMP2
830  00263  106011          LDX     M'37
831  00264  072266          BR      ASGCON
832  00265  106020  SVLBL   LDX     M'30
833  00266  132760  ASGCON  STX     MTX,I
834  00267  132762          STX     MRCV,I
835  00270  114160          AND     TEMP
836  00271  132764          STX     TXTBL,I
837  00272  132766          STX     RCVTBL,I
838  00273  106162          LDX     TEMP2
839  00274  116157          OR      MBIT15
840  00275  132163          STX     TEMP3
841  00276  072354          BR      FORMCW
842  00277  114007  FDVOC   AND     M'1777
843  00300  116155          OR      MBIT13
844  00301  132163          STX     TEMP3
845  00302  132167          STX     TEMP4
846  00303  013004          LDJ     4
847  00304  017737          RS      R
848  00305  177304          BRJ     *-1
849  00306  116156          OR      MBIT14
850  00307  132173          STX     TEMP5
851  00310  106574          LDX     DSWTCH,I
852  00311  162156          TST     MBIT14
853  00312  056317          BREQ    *+5
854  00313  106173          LDX     TEMP5
855  00314  132167          STX     TEMP4
856  00315  106163          LDX     TEMP3
857  00316  132173          STX     TEMP5
858  00317  164163          STZ     TEMP3
859  00320  170004          TDM     FMT
860  00321  042330          BRLT    FDSBLR+2
861  00322  106167          LDX     TEMP4
862  00323  114032          AND     C17777
863  00324  162160          TST     TEMP
864  00325  056332          BREQ    FDLBLR
865  00326  106150  FDSBLR  LDX     MBIT3
866  00327  132162          STX     TEMP2
867  00330  106011          LDX     M'37
868  00331  072333          BR      *+2
869  00332  106020  FDLBLR  LDX     M'30
870  00333  132762          STX     MRCV,I
871  00334  114167          AND     TEMP4
872  00335  132766          STX     RCVTBL,I
873  00336  170004          TDM     FMT
874  00337  042346          BRLT    FDSBLT+2
875  00340  106173          LDX     TEMP5
876  00341  114032          AND     C17777
877  00342  162160          TST     TEMP
878  00343  056350          BREQ    FDLBLT
879  00344  106150  FDSBLT  LDX     MBIT3
880  00345  132163          STX     TEMP3
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881  00346  106011            LDX     M'37
882  00347  072351            BR      *+2
883  00350  106020  FDLBLT    LDX     M'30
884  00351  132760            STX     MTX,I
885  00352  114173            AND     TEMP5
886  00353  132764            STX     TXTBL,I
887  00354  014400  FORMCW     TIX     R
888  00355  011740            INC     R
889  00356  116143            OR      MBIT3
890  00357  132167            STX     TEMP4
891  00360  013003            LDJ     3
892  00361  017677            LS      R
893  00362  177361            BRJ     *-1
894  00363  116167            OR      TEMP4
895  00364  114161            AND     TEMP1
896  00365  116162            OR      TEMP2
897  00366  132772            STX     RCVCW,I
898  00367  120162            XOR     TEMP2
899  00370  116163            OR      TEMP3
900  00371  132770            STX     TXCW,I
901  00372  002043            SRT     3
902                 *START OF INTERRUPT ROUTINES
903                 *INTERRUPT IDENTIFICATION ROUTINE
904  00373  132130  INTID      STX     XSTORE
905  00374  013737            RSC     R
906  00375  132131            STX     CSTORE
907  00376  011257            INP     '17
908  00377  114011            AND     M'37
909  00400  017737            RS      R
910  00401  010100            BRPC    (I)  TSINT
911            001474
912  00403  017737  TSINTR     RS      R
913  00404  050255            BRC     RSINT
914  00405  017737  RSINTR     RS      R
915  00406  050020            BRC     LKINT
916  00407  017737  LKINTR     RS      R
917  00410  050113            BRC     CPINT
918  00411  017737            RS      R
919  00412  010100  CPINTR     BRPC    (I)  ECINT
920            001750
921  00414  100131  INTRTN     LDL     CSTORE
922  00415  106130            LDX     XSTORE
923  00416  006000            IEN     R
924  00417  032040            SRT     0
925                 *LINK INTERRUPT ROUTINE
926  00420  132127  LKINT      STX     SINTWD
927  00421  170217            TDM     LKENBL
928  00422  056106            BREQ    LKIE1
929  00423  013407            LDK     7
930  00424  011250            INP     '10
931  00425  114012            AND     MBYTE
932  00426  132216            STX     RBYTE
933  00427  106227            LDX     RBYTNO
934  00430  011740            INC     R
935  00431  132227            STX     RBYTNO
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936  00432  160140           CMP     MBIT0
937  00433  076037           BRNE    LKINT0
938  00434  106216           LDX     RBYTE
939  00435  132215           STX     RBYTE1
940  00436  072106           BR      LKIE1
941  00437  160141  LKINT0    CMP     MBIT1
942  00440  056047           BREQ    LKINT1
943  00441  106215           LDX     RBYTE1
944  00442  017677           LS      R
945  00443  177442           BRK     *-1
946  00444  116216           OR      RBYTE
947  00445  132317           STX     NCTW2R
948  00446  072105           BR      LKIE1-1
949  00447  106216  LKINT1    LDX     RBYTE
950  00450  017677           LS      R
951  00451  177450           BRK     *-1
952  00452  116215           OR      RBYTE1
953  00453  132177           STX     ITEMP
954  00454  106230           LDX     LWCNTR
955  00455  003400           TXK     R
956  00456  011740           INC     R
957  00457  132230           STX     LWCNTR
958  00460  112141           SUB     MBIT1
959  00461  132234           STX     LINKF
960  00462  106177           LDX     ITEMP
961  00463  133714           STX     NRLKWD,K
962  00464  105710           LDC     LSADR,K
963  00465  056106           BREQ    LKIE1
964  00466  106177  LKINT2    LDX     ITEMP
965  00467  170216           TDM     RBYTE
966  00470  076072           BRNE    *+2
967  00471  001763           CLX     R
968  00472  004000           OUT     0
969  00473  106230           LDX     LWCNTR
970  00474  017677           LS      R
971  00475  017677           LS      R
972  00476  017677           LS      R
973  00477  116200           OR      HORCNT
974  00500  017677           LS      R
975  00501  017677           LS      R
976  00502  017677           LS      R
977  00503  017677           LS      R
978  00504  133710           STX     LSADR,K
979  00505  164227           STZ     RBYTNO
980  00506  106142  LKIE1     LDX     MBIT2
981  00507  004017           OUT     '17
982  00510  106127           LDX     SINTWD
983  00511  056014           BREQ    INTRTN
984  00512  072007           BR      LKINTR
985                 *CORRELATION PROCESSOR INTERRUPT ROUTINE
986  00513  132127  CPINT     STX     SINTWD
987  00514  170220           TDM     CPENBL
988  00515  056251           BREQ    CPIE
989  00516  011252  A/DINP    INP     '12
990  00517  042122           BRLT    *+3
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 991  00520  114013          AND     M*3777
 992  00521  072123          BR      *+2
 993  00522  116031          OR      C*3777
 994  00523  001760          CMX     R
 995  00524  011740          INC     R
 996  00525  132177          STX     ITEMP
 997  00526  106176          LDX     SWITCH
 998  00527  162154          TST     MBIT12
 999  00530  056206          BREQ    CPINT6
1000  00531  106177          LDX     ITEMP
1001  00532  160226          CMP     SPSUM
1002  00533  042141          BRLT    CPINT1
1003  00534  132226          STX     SPSUM
1004  00535  106215          LDX     SCNT
1005  00536  114011          AND     MSUBFR
1006  00537  132216          STX     SRSLOT
1007  00540  164221          STZ     OVRINC
1008  00541  106230  CPINT1  LDY     PCNT
1009  00542  160011          CMP     PCNTMX
1010  00543  062150          BRGE    CPINT2
1011  00544  011740          INC     R
1012  00545  132230          STX     PCNT
1013  00546  106140          LDX     MBIT0
1014  00547  072160          BR      CPINT3
1015  00550  164230  CPINT2  STZ     PCNT
1016  00551  106227          LDX     DCNTR
1017  00552  160063          CMP     DCNTMX
1018  00553  066163          BRGT    CPINT4
1019  00554  106221          LDX     OVRINC
1020  00555  110062          ADD     SCHINC
1021  00556  132221          STX     OVRINC
1022  00557  106141          LDX     MBIT1
1023  00560  110215  CPINT3  ADD     SCNT
1024  00561  132215          STX     SCNT
1025  00562  072251          BR      CPIE
1026  00563  106226  CPINT4  LDX     SPSUM
1027  00564  160064          CMP     CLAGTH
1028  00565  066171          BRGT    CRSCOR
1029  00566  106034          LDX     M*1700
1030  00567  114176          AND     SWITCH
1031  00570  072204          BR      CPINT5+3
1032  00571  106221  CRSCOR  LDX     OVRINC
1033  00572  112017          SUB     M*7777
1034  00573  046201          BRLE    CPINT5
1035  00574  132221          STX     OVRINC
1036  00575  106017          LDX     M*7777
1037  00576  004012          OUT     *12
1038  00577  106143          LDX     MBIT3
1039  00600  132213          STX     RCVRPT
1040  00601  104154  CPINT5  LDC     MBIT12
1041  00602  114176          AND     SWITCH
1042  00603  116153          OR      MBIT11
1043  00604  132176          STX     SWITCH
1044  00605  072251          BR      CPIE
1045  00606  106222  CPINT6  LDX     CLPNTR
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1046  00607  056236          BREQ    CPINT7
1047  00610  017677          LS      R
1048  00611  132222          STX     CLPNTR
1049  00612  162141          TST     MBIT1
1050  00613  056220          BREQ    INPCD-2
1051  00614  106177  INPCS   LDX     ITEMP
1052  00615  110246          ADD     CCSUM
1053  00616  132246          STX     CCSUM
1054  00617  072251          BR      CPIE
1055  00620  162142          TST     MBIT2
1056  00621  056230          BREQ    INPCS0
1057  00622  106177  INPCD   LDX     ITEMP
1058  00623  110247          ADD     CCDIF
1059  00624  132247          STX     CCDIF
1060  00625  170222          TDM     CLPNTR
1061  00626  042251          BRLT    CPIE
1062  00627  072233          BR      CPINT7-3
1063  00630  106177  INPCS0  LDX     ITEMP
1064  00631  132224          STX     C/SUM0
1065  00632  166225          STO     SOFLG
1066  00633  164222          STZ     CLPNTR
1067  00634  166232          STO     CLKLPF
1068  00635  072251          BR      CPIE
1069  00636  106177  CPINT7  LDX     ITEMP
1070  00637  170223          TDM     RNGTYP
1071  00640  056244          BREQ    INPRD
1072  00641  164223          STZ     RNGTYP
1073  00642  132257  INPRS   STX     RSUM
1074  00643  072251          BR      CPIE
1075  00644  132261  INPRD   STX     RDIF
1076  00645  106275          LDX     RPTXED
1077  00646  164275          STZ     RPTXED
1078  00647  062251          BRGE    *+2
1079  00650  166233          STO     RNGLPF
1080  00651  106143  CPIE    LDX     MBIT3
1081  00652  004017          OUT     *17
1082  00653  102127          LDR     SINTWD
1083  00654  072012          BR      CPINTR
1084                  *RECEIVE SLOT INTERRUPT ROUTINE
1085  00655  132127  RSINT   STX     SINTWD
1086  00656  106141          LDX     MBIT1
1087  00657  004017          OUT     *17
1088  00660  106201          LDX     RCNTR
1089  00661  011740          INC     R
1090  00662  114044          AND     MFMT
1091  00663  132201          STX     RCNTR
1092  00664  114011          AND     MSUBFR
1093  00665  132202          STX     RSLOT
1094  00666  016141          BRSEQ   TXOVHD+1
1095                  001413
1096  00670  104202          LDC     RSLOT
1097  00671  114011          AND     MSUBFR
1098  00672  160141          CMP     MBIT1
1099  00673  066323          BRGT    DSPLY1
1100  00674  003400          TXH     R
```

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1101  00675  160141          CMP       MBIT1
1102  00676  042307          BRLT      DEVLMP
1103  00677  106166  LPLMP   LDX       LAMPS
1104  00700  004002          OUT       *2
1105  00701  011242          INP       *2
1106  00702  162150          TST       MBIT8
1107  00703  026100          BRPGT (I) INIT
1108         002724
1109  00705  114016          AND       MLPSW
1110  00706  072314          BR        SWTCH
1111  00707  004007  DEVLMP   OUT       *7
1112  00710  107564          LDX       DLAMPS,K
1113  00711  004011          OUT       *11
1114  00712  011251          INP       *11
1115  00713  114011          AND       MDEVSW
1116  00714  132177  SWTCH   STX       ITEMP
1117  00715  105570          LDC       SWFLGS,K
1118  00716  114177          AND       ITEMP
1119  00717  117574          OR        DSWTCH,K
1120  00720  133574          STX       DSWTCH,K
1121  00721  106177          LDX       ITEMP
1122  00722  133570          STX       SWFLGS,K
1123  00723  106176  DSPLY1  LDX       SWITCH
1124  00724  162146          TST       MBIT6
1125  00725  066342          BRGT      DSPLY3
1126  00726  162151          TST       MBIT9
1127  00727  056352          BREQ      DSPLY4
1128  00730  162147          TST       MBIT7
1129  00731  056362          BREQ      RSYNC?
1130  00732  120147          XOR       MBIT7
1131  00733  132176          STX       SWITCH
1132  00734  011241          INP       *1
1133  00735  136132          STD       MEMADR
1134  00736  104151  DSPLY2  LDC       MBIT9
1135  00737  114176          AND       SWITCH
1136  00740  132176          STX       SWITCH
1137  00741  072362          BR        RSYNC?
1138  00742  104021  DSPLY3  LDC       M*300
1139  00743  114176          AND       SWITCH
1140  00744  116151          OR        MBIT9
1141  00745  132176          STX       SWITCH
1142  00746  011241          INP       *1
1143  00747  056336          BREQ      DSPLY2
1144  00750  132132          STX       MEMADR
1145  00751  072361          BR        RSYNC?-1
1146  00752  106201  DSPLY4  LDX       RCNTR
1147  00753  114036          AND       MDSPLY
1148  00754  160057          CMP       DSPLYT
1149  00755  076362          BRNE      RSYNC?
1150  00756  011241          INP       *1
1151  00757  132177          STX       DSPADR
1152  00760  134177          LDD       DSPADR
1153  00761  004001          OUT       *1
1154  00762  106201  RSYNC?  LDX       RCNTR
1155  00763  114040          AND       MRSYNC
```

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1156  00764   160041          CMP       RSYNCT
1157  00765   076370          BRNE      *+3
1158  00766   106155          LDX       MBIT13
1159  00767   004016          OUT       '16
1160  00770   106213          LDX       RCVRPT
1161  00771   056377          BREQ      CLCT1
1162  00772   017757          DEC       R
1163  00773   132213          STX       RCVRPT
1164  00774   106214          LDX       SRCVCW
1165  00775   032100          BRP   (I) RSIE3
1166          001352
1167  00777   106176  CLCT1   LDX       SWITCH
1168  01000   162152          TST       MBIT10
1169  01001   066066          BRGT      RLCT1
1170  01002   162153          TST       MBIT11
1171  01003   066047          BRGT      CLCT3
1172  01004   162154          TST       MBIT12
1173  01005   066030          BRGT      CLCT2
1174  01006   011242          INP       '2
1175  01007   162141          TST       MBIT1
1176  01010   056350          BREQ      RSIE1
1177  01011   106176          LDX       SWITCH
1178  01012   116154          OR        MBIT12
1179  01013   132176          STX       SWITCH
1180  01014   104266          LDC       TXCLKF
1181  01015   114013          AND       M'3777
1182  01016   120152          XOR       MBIT10
1183  01017   116005          OR        M'17
1184  01020   120140          XOR       MBITC
1185  01021   132166          STX       LAMPS
1186  01022   106202          LDX       RSLOT
1187  01023   011740          INC       R
1188  01024   132215          STX       SCNT
1189  01025   166265          STO       CLINIT
1190  01026   106044          LDX       MFMT
1191  01027   072347          BR        RSIE1-1
1192  01030   106227  CLCT2   LDX       DCNTR
1193  01031   011740          INC       R
1194  01032   132227          STX       DCNTR
1195  01033   160063          CMP       DCNTMX
1196  01034   066064          BRGT      CLCT4
1197  01035   106062          LDX       SCHINC
1198  01036   120157          XOR       MBIT15
1199  01037   004012          OUT       '12
1200  01040   166220          STO       CPENBL
1201  01041   106145          LDX       MBIT5
1202  01042   132213          STX       RCVRPT
1203  01043   106053          LDX       CSOCW
1204  01044   132214          STX       SRCVCW
1205  01045   001763          CLX       R
1206  01046   072353          BR        RSIE3+1
1207  01047   106202  CLCT3   LDX       RSLOT
1208  01050   160216          CMP       SRSLOT
1209  01051   076350          BRNE      RSIE1
1210  01052   164201          STZ       RCNTR
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1211  01053  166245          STO     NUMAV
1212  01054  106176          LDX     SWITCH
1213  01055  120153          XOR     MBIT11
1214  01056  116152          OR      MBIT10
1215  01057  132176          STX     SWITCH
1216  01060  106141          LDX     MBIT1
1217  01061  132252          STX     CLPC
1218  01062  106221          LDX     OVRINC
1219  01063  004012          OUT     *12
1220  01064  106143  CLCT4   LDX     MBIT3
1221  01065  072347          BR      RSIE1-1
1222  01066  170274  RLCT1   TDM     TXACQF
1223  01067  046157          BRLE    RLCT9
1224  01070  170272          TDM     RLTRK
1225  01071  046157          BRLE    RLCT9
1226  01072  106143          LDX     CRADR
1227  01073  110011          ADD     M*37
1228  01074  160201          CMP     RCNTR
1229  01075  056104          BREQ    RLCT3
1230  01076  106201          LDX     RCNTR
1231  01077  160143          CMP     CRADR
1232  01100  076157          BRNE    RLCT9
1233  01101  106236  RLCT2   LDX     RCWMOD
1234  01102  116152          OR      MBIT10
1235  01103  072155          BR      RLCT8+2
1236  01104  170275  RLCT3   TDM     RPTXED
1237  01105  046153          BRLE    RLCT8
1238  01106  164275          STZ     RPTXED
1239  01107  011256          INP     *16
1240  01110  114140          AND     MBIT0
1241  01111  076116          BRNE    RLCT4
1242  01112  106277          LDX     CRTC
1243  01113  011740          INC     R
1244  01114  132277          STX     CRTC
1245  01115  072120          BR      RLCT4+2
1246  01116  170277  RLCT4   TDM     CRTC
1247  01117  056132          BREQ    RLCT5
1248  01120  106301          LDX     CRPC
1249  01121  011740          INC     R
1250  01122  132301          STX     CRPC
1251  01123  160115          CMP     CRPCMX
1252  01124  042153          BRLT    RLCT8
1253  01125  106277          LDX     CRTC
1254  01126  160116          CMP     CRTCMN
1255  01127  062141          BRGE    RLCT6
1256  01130  164277          STZ     CRTC
1257  01131  164301          STZ     CRPC
1258  01132  106257  RLCT5   LDX     CRSC
1259  01133  017757          DEC     R
1260  01134  046147          BRLE    RLCT7
1261  01135  132257          STX     CRSC
1262  01136  106113          LDX     CRSINC
1263  01137  132251          STX     RLCORR
1264  01140  072153          BR      RLCT8
1265  01141  166274  RLCT6   STO     TXACQF
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1266  01142  106166          LDX     LAMPS
1267  01143  120145          XOR     MBIT5
1268  01144  120146          XOR     MBIT6
1269  01145  132166          STX     LAMPS
1270  01146  072136          BR      RLCT5+4
1271  01147  164274  RLCT7    STZ     TXACGF
1272  01150  106166          LDX     LAMPS
1273  01151  116144          OR      MBIT4
1274  01152  132166          STX     LAMPS
1275  01153  106033  RLCT8    LDX     C37777
1276  01154  114236          AND     PCWMOD
1277  01155  132236          STX     PCWMOD
1278  01156  072170          BR      RSLT01
1279  01157  106202  RLCT9    LDX     RSLOT
1280  01160  160035          CMP     D24
1281  01161  076171          BRNE    RSLT01+1
1282  01162  106251          LDX     RLCORR
1283  01163  056170          BREQ    RSLT01
1284  01164  132375          STX     RLCOR1
1285  01165  116154          OR      MBIT12
1286  01166  004012          OUT     *12
1287  01167  164251          STZ     RLCORR
1288  01170  106202  RSLT01  LDX     RSLOT
1289  01171  076251          BRNE    RCVD1
1290  01172  170240          TDM     ENRCV
1291  01173  046175          BRLE    *+2
1292  01174  166240          STO     RCVEN
1293  01175  164227          STZ     RBYTNO
1294  01176  164310          STZ     LSADR
1295  01177  164230          STZ     LWCNTR
1296  01200  106201          LDX     RCNTR
1297  01201  132200          STX     HORCNT
1298  01202  076216          BRNE    DPTST
1299  01203  106266          LDX     TXCLKF
1300  01204  116241          OR      RDRNGF
1301  01205  056216          BREQ    DPTST
1302  01206  011253  RDRNG    INP     *13
1303  01207  114047          AND     MRANGE
1304  01210  132211          STX     RANGE2
1305  01211  106203          LDX     TCNTR
1306  01212  132210          STX     RANGE1
1307  01213  170241          TDM     RDRNGF
1308  01214  026141          BRSGT   SCHREQ,1
1309         001470
1310  01216  170242  DPTST    TDM     DPFLG
1311  01217  042240          BRLT    RSLT04
1312  01220  170237          TDM     CLFLG
1313  01221  062231          BRGE    RSLT02
1314  01222  170201          TDM     RCNTR
1315  01223  056283          BREQ    RSLT03
1316  01224  170212          TDM     CTLWTF
1317  01225  062231          BRGE    RSLT02
1318  01226  106142          LDX     MBIT2
1319  01227  004000          OUT     *0
1320  01230  164207          STZ     ECWDOF
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1321  01231  106140  RSLT02   LDX          MBIT0
1322  01232  072245           BR           RSLT05
1323  01233  106052  RSLT03   LDX          SOFCW
1324  01234  004000           OUT          *0
1325  01235  166217           STO          LKENBL
1326  01236  106140           LDX          MBIT0
1327  01237  132230           STX          LWCNTR
1328  01240  106056  RSLT04   LDX          CSOCW
1329  01241  132214           STX          SRCVCW
1330  01242  106140           LDX          MBIT0
1331  01243  132213           STX          RCVRPT
1332  01244  116155           OR           MBIT13
1333  01245  132222  RSLT05   STX          CLPNTR
1334  01246  106053           LDX          CSOCW
1335  01247  116155           OR           MBIT13
1336  01250  072352           BR           RSIE3
1337  01251  170240  RCVD1    TDM          RCVEN
1338  01252  062350           BRGE         RSIE1
1339  01253  160143           CMP          MBIT5
1340  01254  062323           BRGE         RSLT0
1341  01255  106140           LDX          MBIT0
1342  01256  132213           STX          RCVRPT
1343  01257  106201           LDX          RCNTR
1344  01260  160134           CMP          LKADR
1345  01261  076313           BRNE         NCTTST
1346  01262  170266  LKRNG    TDM          TXCLKF
1347  01263  042342           BRLT         NCT2
1348  01264  106176           LDX          SWITCH
1349  01265  114022           AND          M*60
1350  01266  076270           BRNE         *+2
1351  01267  170374           TDM          DLYC
1352  01270  026100           BRPGT (I)    INITRL
1353         002577
1354  01272  166223           STO          RNGTYP
1355  01273  170274           TDM          TXACQF
1356  01274  062342           BRGE         NCT2
1357  01275  170251           TDM          RLCORR
1358  01276  076342           BRNE         NCT2
1359  01277  106272           LDX          RLTRK
1360  01300  056342           BREQ         NCT2
1361  01301  042306  TSTRP    BRLT         RPCONT
1362  01302  106054           LDX          S/DMOD
1363  01303  132214           STX          SRCVCW
1364  01304  106153           LDX          MBIT11
1365  01305  072352           BR           RSIE3
1366  01306  106054  RPCONT   LDX          S/DMOD
1367  01307  116055           OR           LNKBCW
1368  01310  132214           STX          SRCVCW
1369  01311  106055           LDX          LNKBCW
1370  01312  072352           BR           RSIE3
1371  01313  017757  NCTTST   DEC          R
1372  01314  162046           TST          MYCTID
1373  01315  056335           BREQ         NCT1
1374  01316  160140           CMP          MBIT0
1375  01317  056350           BREQ         RSIE1
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1376  01320  162011          TST       MSUBFR
1377  01321  076342          BRNE      NCT2
1378  01322  164213          STZ       RCVRPT
1379  01323  013401  RSLTD   LDK       1
1380  01324  106201          LDX       RCNTR
1381  01325  115762          AND       MRCV,K
1382  01326  161766          CMP       RCVTBL,K
1383  01327  056332          BREQ      *+3
1384  01330  177724          BRK       RSLTD+1
1385  01331  072350          BR        RSIE1
1386  01332  107772          LDX       RCVCW,K
1387  01333  056330          BREQ      *-3
1388  01334  072352          BR        RSIE3
1389  01335  160135  NCT1    CMP       NCTSLT
1390  01336  076344          BRNE      NCT3
1391  01337  166310          STO       LSADR
1392  01340  106141          LDX       MBIT1
1393  01341  132213          STX       RCVRPT
1394  01342  106055  NCT2    LDX       LNKBCW
1395  01343  072351          BR        RSIE2
1396  01344  106140  NCT3    LDX       MBIT0
1397  01345  132200          STX       LWCNTR
1398  01346  106141          LDX       MBIT1
1399  01347  132213          STX       RCVRPT
1400  01350  001763  RSIE1    CLX       R
1401  01351  132214  RSIE2    STX       SRCVCW
1402  01352  116236  RSIE3    OR        RCWMOD
1403  01353  004014          OUT       '14
1404  01354  106127  RSIE4    LDX       SINTWD
1405  01355  016100          BRPEQ (I) INTRTN
1406         000414
1407  01357  032100          BRP   (I) RSINTR
1408         000405
1409                  *INITIALIZE (SET TO ZERO) BLOCK STORAGE
1410  01361  132161  STZBS    STX       DMADMX     SUBROUTINE
1411  01362  001763          CLX       R
1412  01363  136160          STD       DMADR
1413  01364  106160          LDX       DMADR
1414  01365  160161          CMP       DMADMX
1415  01366  022043          SRTGE     3
1416  01367  011740          INC       R
1417  01370  132160          STX       DMADR
1418  01371  072362          BR        STZBS+1
1419                  *TRANSMIT TIMING INITIALIZATION SUBROUTINE
1420  01372  110201  INITTX   ADD       RCNTR
1421  01373  011740          INC       R
1422  01374  114044          AND       MFMT
1423  01375  132203          STX       TCNTR
1424  01376  164270          STZ       STXCW
1425  01377  106157          LDX       MBIT15
1426  01400  004016          OUT       '16
1427  01401  004015          OUT       '15
1428  01402  106140          LDX       MBIT0
1429  01403  004017          OUT       '17
1430  01404  106177          LDX       ITEMP
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1431  01405  004013            OUT       #13
1432  01406  160050            CMP       RORNG
1433  01407  036041            SRTNE     1
1434  01410  106156            LDX       MBIT14
1435  01411  004016            OUT       #16
1436  01412  032041            SRT       1
1437                  *TRANSMIT OVERHEAD SUBROUTINE
1438  01413  106374  TXOVHD    LDX       DLYC
1439  01414  046024            BRLE      CLKTST
1440  01415  017757            DEC       R
1441  01416  132374            STX       DLYC
1442  01417  066024            BRGT      CLKTST
1443  01420  104005            LDC       M#17
1444  01421  116166            OR        LAMPS
1445  01422  120152            XOR       MBIT10
1446  01423  132166            STX       LAMPS
1447  01424  011242  CLKTST    INP       2
1448  01425  162140            TST       MBIT0
1449  01426  076053            BRNE      TXCLK
1450  01427  170266  TSTCKF    TDM       TXCLKF
1451  01430  016041            SRTEQ     1
1452  01431  164266            STZ       TXCLKF
1453  01432  170251            TDM       CLTRK
1454  01433  062070            BRGE      SCHREQ
1455  01434  166241            STO       RDRNGF
1456  01435  166272            STO       RLTRK
1457  01436  166273            STO       RLFLG
1458  01437  166274            STO       TXACQF
1459  01440  166265            STO       RLAQF
1460  01441  164263            STZ       RLSCHI
1461  01442  164275            STZ       RPTXED
1462  01443  106105            LDX       VRLCMX
1463  01444  132301            STX       VRLC
1464  01445  106106            LDX       RLTCMN
1465  01446  132277            STX       RLTC
1466  01447  170271            TDM       TXEN
1467  01450  002041            SRTLT     1
1468  01451  132271            STX       ENTX
1469  01452  032041            SRT       1
1470  01453  170266  TXCLK     TDM       TXCLKF
1471  01454  002041            SRTLT     1
1472  01455  166266            STO       TXCLKF
1473  01456  164272            STZ       RLTRK
1474  01457  164241            STZ       RDRNGF
1475  01460  164374            STZ       DLYC
1476  01461  106005            LDX       M#17
1477  01462  114166            AND       LAMPS
1478  01463  116152            OR        MBIT10
1479  01464  132166            STX       LAMPS
1480  01465  170271            TDM       TXEN
1481  01466  002041            SRTLT     1
1482  01467  132271            STX       ENTX
1483  01470  106034  SCHREQ    LDX       M#1700
1484  01471  114176            AND       SWITCH
1485  01472  132176            STX       SWITCH
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1486  01473  032041                SRT     1
1487                 *TRANSMIT SLOT INTERRUPT ROUTINE
1488  01474  132127  TSINT         STX     SINTWD
1489  01475  106140                LDX     MBIT0
1490  01476  004017                OUT     *17
1491  01477  106203                LDX     TCNTR
1492  01500  011740                INC     R
1493  01501  114044                AND     MFMT
1494  01502  132203                STX     TCNTR
1495  01503  114011                AND     MSUBFR
1496  01504  132204                STX     TSLOT
1497  01505  106203                LDX     TCNTR
1498  01506  114042                AND     MTSYNC
1499  01507  160043                CMP     TSYNCT
1500  01510  076113                BRNE    *+3
1501  01511  106154                LDX     MBIT12
1502  01512  004016                OUT     *16
1503  01513  106267                LDX     TXRPT
1504  01514  056121                BREQ    TXCK?
1505  01515  017757                DEC     R
1506  01516  132267                STX     TXRPT
1507  01517  106270                LDX     STXCW
1508  01520  072342                BR      TSIE1+2
1509  01521  170266  TXCK?         TDM     TXCLKF
1510  01522  042157                BRLT    TSINT1
1511  01523  011242                INP     2
1512  01524  114143                AND     MBIT3
1513  01525  066337                BRGT    TSIE0+1
1514  01526  170231  TSTCL         TDM     CLTRK
1515  01527  062336                BRGE    TSIE0
1516  01530  106272  TSTRL         LDX     RLTRK
1517  01531  042157                BRLT    TSINT1
1518  01532  056336                BREQ    TSIE0
1519  01533  170252                TDM     CLPC
1520  01534  066340                BRGT    TSIE1
1521  01535  106203                LDX     TCNTR
1522  01536  170274                TDM     TXACQF
1523  01537  066150                BRGT    CRSRNG
1524  01540  160134  FNPNG         CMP     LRADR
1525  01541  076336                BRNE    TSIE0
1526  01542  106140                LDX     MBIT0
1527  01543  132267                STX     TXRPT
1528  01544  166275                STO     RPTXED
1529  01545  164270                STZ     STXCW
1530  01546  106153                LDX     MBIT11
1531  01547  072342                BR      TSIE1+2
1532  01550  160133  CRSRNG        CMP     CRADR
1533  01551  076336                BRNE    TSIE0
1534  01552  106041                LDX     M*37
1535  01553  132267                STX     TXRPT
1536  01554  132275                STX     RPTXED
1537  01555  106152                LDX     MBIT10
1538  01556  072341                BR      TSIE1+1
1539  01557  170271  TSINT1        TDM     TXEN
1540  01560  042174                BRLT    TSINT2
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1541  01561  106204           LDX     TSLOT
1542  01562  076340           BRNE    TSIE1
1543  01563  170271           TDM     ENTX
1544  01564  056340           BREQ    TSIE1
1545  01565  166271           STO     TXEN
1546  01566  170212           TDM     CTLWCT
1547  01567  042172           BRLT    *+3
1548  01570  106141           LDX     MBIT1
1549  01571  132212           STX     CTLWCT
1550  01572  164303           STZ     TXLWPT
1551  01573  164302           STZ     TXLWCT
1552  01574  106204  TSINT2   LDX     TSLOT
1553  01575  170266           TDM     TXCLKF
1554  01576  056206           BREQ    TSINT3
1555  01577  076206           BRNE    TSINT3
1556  01600  170203  TSLT01   TDM     TCNTR
1557  01601  076204           BRNE    TSLT02
1558  01602  106140           LDX     MBIT0
1559  01603  132267           STX     TXRPT
1560  01604  106151  TSLT02   LDX     MBIT9
1561  01605  072341           BR      TSIE1+1
1562  01606  160140  TSINT3   CMP     MBIT0
1563  01607  056267           BREQ    TSLT11
1564  01610  160143           CMP     MBIT3
1565  01611  062317           BRGE    TSLT0
1566  01612  106203           LDX     TCNTR
1567  01613  160134           CMP     LRADR
1568  01614  076340           BRNE    TSIE1
1569  01615  102303  TLNK0    LDR     TXLWPT
1570  01616  003400           TXK     R
1571  01617  114156           AND     MBIT14
1572  01620  056227           BREQ    TLNK1
1573  01621  107704           LDX     AKLKWD,K
1574  01622  032141           BRS     LKWDCT,1
1575         000127
1576  01624  076263           BRNE    TLNK4
1577  01625  165704           STZ     AKLKWD,K
1578  01626  072242           BR      TLNK2-6
1579  01627  004010  TLNK1    OUT     *10
1580  01630  050250           BRC     TLNK2
1581  01631  107750           LDX     TLKWD1,K
1582  01632  076244           BRNE    *+10
1583  01633  107704           LDX     AKLKWD,K
1584  01634  056242           BREQ    *+6
1585  01635  032141           BRS     LKWDCT,1
1586         000127
1587  01637  106303           LDX     TXLWPT
1588  01640  116157           OR      MBIT15
1589  01641  072262           BR      TLNK4-1
1590  01642  106141           LDX     MBIT1
1591  01643  072260           BR      TLNK3+1
1592  01644  032141           BRS     LKWDCT,1
1593         000127
1594  01646  076263           BRNE    TLNK4
1595  01647  072257           BR      TLNK3
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1596  01650  107752  TLNK2   LDX     TLKWD2,K
1597  01651  056256          BREQ    TLNK3-1
1598  01652  032141          BRS     LKWDCT,1
1599         000127
1600  01654  076263          BRNE    TLNK4
1601  01655  165752          STZ     TLKWD2,K
1602  01656  165750          STZ     TLKWD1,K
1603  01657  106140  TLNK3   LDX     MBIT0
1604  01660  110303          ADD     TXLWPT
1605  01661  114010          AND     M'3
1606  01662  132303          STX     TXLWPT
1607  01663  104266  TLNK4   LDC     TXCLKF
1608  01664  132275          STX     RPTXED
1609  01665  106140          LDX     MBIT0
1610  01666  072312          BR      TSLT12+4
1611  01667  106203  TSLT11  LDX     TCNTR
1612  01670  017757          DEC     R
1613  01671  160135          CMP     NCTSLT
1614  01672  076315          BRNE    TSLT13
1615  01673  011243          INP     3
1616  01674  162151          TST     MBIT9
1617  01675  056340          BREQ    TSIE1
1618  01676  106212          LDX     CTLWCT
1619  01677  042306          BRLT    TSLT12
1620  01700  017757          DEC     R
1621  01701  132212          STX     CTLWCT
1622  01702  106205          LDX     ECWD0
1623  01703  004010          OUT     '10
1624  01704  106206          LDX     ECWD1
1625  01705  072310          BR      TSLT12+2
1626  01706  001763  TSLT12  CLX     R
1627  01707  004010          OUT     '10
1628  01710  004006          OUT     '6
1629  01711  106141          LDX     MBIT1
1630  01712  132267          STX     TXRPI
1631  01713  106055          LDX     LNKSCW
1632  01714  072341          BR      TSIE1+1
1633  01715  114046  TSLT13  AND     MNCTLD
1634  01716  056340          BREQ    TSIE1
1635  01717  013401  TSLTD   LDK     1
1636  01720  106203          LDX     TCNTR
1637  01721  115760          AND     MTX,K
1638  01722  161764          CMP     TXTBL,K
1639  01723  056326          BREQ    *+3
1640  01724  177720          BRK     TSLTD+1
1641  01725  072340          BR      TSIE1
1642  01726  107770          LDX     TXCW,K
1643  01727  056324          BREQ    *-3
1644  01730  066342          BRGT    TSIE1+2
1645  01731  107574          LDX     DSWTCH,K
1646  01732  162152          TST     MBIT10
1647  01733  076340          BRNE    TSIE1
1648  01734  107770          LDX     TXCW,K
1649  01735  072342          BR      TSIE1+2
1650  01736  106014  TSIE0   LDX     M'7
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1651  01737  132271                STX        ENTX
1652  01740  001763  TSIE1       CLX        R
1653  01741  132270                STX        STXCW
1654  01742  004015                OUT        •15
1655  01743  106127                LDX        SINTWD
1656  01744  016100                BRPEQ (I)  INTRTN
1657         000414
1658  01746  032100                BRP   (I)  TSINTR
1659         000403
1660                  *EXTERNAL COMPUTER INTERRUPT ROUTINE
1661  01750  011240  ECINT        INP        0
1662  01751  001760                CMX        R
1663  01752  170207                TDM        ECWD0F
1664  01753  062360                BRGE       ECINT0
1665  01754  132206                STX        ECWD1
1666  01755  106141                LDX        MBIT1
1667  01756  132212                STX        CILWCT
1668  01757  072365                BR         ECINT1
1669  01760  166207  ECINT0       STO        ECWD0F
1670  01761  132205                STX        ECWD0
1671  01762  106142                LDX        MBIT2
1672  01763  011740                INC        R
1673  01764  004000                OUT        0
1674  01765  106144  ECINT1       LDX        MBIT4
1675  01766  004017                OUT        •17
1676  01767  032100                BRP   (I)  INTRTN
1677         000414
1678                  *SEARCH SUBROUTINE
1679  01771  107254  SEARCH       LDX        SRCHCT,J
1680  01772  017757                DEC        R
1681  01773  133254                STX        SRCHCT,J
1682  01774  107262                LDX        SRCH,J
1683  01775  110062                ADD        SCHINC
1684  01776  120157                XOR        MBIT15
1685  01777  133262                STX        SRCH,J
1686  02000  171254                TDM        SRCHCT,J
1687  02001  026043                SRTGT      3
1688  02002  017737                RS         R
1689  02003  162156                TST        MBIT14
1690  02004  056006                BREQ       *+2
1691  02005  120033                XOR        C37777
1692  02006  165262                STZ        SRCH,J
1693  02007  032043                SRT        3
1694                  *CLOCK LOOP ROUTINE
1695  02010  164232  CLROUT       STZ        CLKLPF
1696  02011  104225                LDC        SOFLG
1697  02012  164225                STZ        SOFLG
1698  02013  116252                OR         CLPC
1699  02014  076071                BRNE       CLROU1
1700  02015  106256                LDX        SCCSUM
1701  02016  132162                STX        MCND
1702  02017  170242                TDM        OPFLG
1703  02020  042045                BRLT       DBLP1
1704  02021  106101                LDX        SAPVTM
1705  02022  032143                BRS        MULT,3
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1706                 002345
1707   02024         160224          CMP       C/SUMO
1708   02025         062033          BRGE      DBLP0
1709   02026         166243          STO       FRMLK
1710   02027         164244          STZ       LOFC
1711   02030         104142          LDC       MBIT2
1712   02031         114166          AND       LAMPS
1713   02032         072043          BR        DBLP1-2
1714   02033         106244  DBLP0   LDX       LOFC
1715   02034         011740          INC       R
1716   02035         102243          STX       FRMLK
1717   02036         160077          CMP       LOFCMX
1718   02037         062305          BRGE      REQSCH
1719   02040         132244          STX       LOFC
1720   02041         106166          LDX       LAMPS
1721   02042         116142          OR        MBIT2
1722   02043         132166          STX       LAMPS
1723   02044         072071          BR        CLROU1
1724   02045         106100  DBLP1   LDX       SUPATM
1725   02046         032143          BRS       MULT*3
1726                 002345
1727   02050         160224          CMP       C/SUMO
1728   02051         062062          BRGE      DBLP2
1729   02052         010000          IDS       R
1730   02053         106202          LDX       RSLOT
1731   02054         132201          STX       RCNTR
1732   02055         006000          IEN       R
1733   02056         132243          STX       FRMLK
1734   02057         164244          STZ       LOFC
1735   02060         132242          STX       DPFLG
1736   02061         072071          BR        CLROU1
1737   02062         106200  DBLP2   LDX       HORCNT
1738   02063         076071          BRNE      CLROU1
1739   02064         106244          LDX       SFCT
1740   02065         011740          INC       R
1741   02066         160076          CMP       SFCTMX
1742   02067         062335          BRGE      REQSCH
1743   02070         132244          STX       SFCT
1744   02071         106245  CLROU1  LDX       NUMAV
1745   02072         062107          BRGE      CLROU2
1746   02073         106071          LDX       AVNUM
1747   02074         132162          STX       MCND
1748   02075         106226          LDX       SPSUM
1749   02076         032143          BRS       MULT*3
1750                 002345
1751   02100         102163          LDR       MPLR
1752   02101         132162          STX       MCND
1753   02102         106072          LDX       CLATM
1754   02103         032143          BRS       MULT*3
1755                 002345
1756   02105         132226          STX       FNLKTH
1757   02106         001763          CLX       R
1758   02107         011740  CLROU2  INC       R
1759   02110         132245          STX       NUMAV
1760   02111         160071          CMP       AVNUM
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1761  02112  042343          BRLT    CLEXIT
1762  02113  164245          STZ     NUMAV
1763  02114  013000          LDJ     0
1764  02115  106247          LDX     CCDIF
1765  02116  132260          STX     SCCDIF
1766  02117  164247          STZ     CCDIF
1767  02120  106246          LDX     CCSUM
1768  02121  062123          BRGE    *+2
1769  02122  001763          CLX     K
1770  02123  132256          STX     SCCSUM
1771  02124  164246          STZ     CCSUM
1772  02125  112226          SUB     FNLKTH
1773  02126  132160          STX     TEMP
1774  02127  026142          BRSGT   CORR,2
1775         002360
1776  02131  106160          LDX     TEMP
1777  02132  170237          TDM     CLFLG
1778  02133  056242          BREQ    CLTST1
1779  02134  066140          BRGT    *+4
1780  02135  104156          LDC     MBIT14
1781  02136  114236          AND     RCWMOD
1782  02137  072145          BR      *+6
1783  02140  106276          LDX     CLTC
1784  02141  017757          DEC     R
1785  02142  132276          STX     CLTC
1786  02143  106053          LDX     C37777
1787  02144  116236          OR      RCWMOD
1788  02145  132236          STX     RCWMOD
1789  02146  106300          LDX     VCLC
1790  02147  017757          DEC     R
1791  02150  132300          STX     VCLC
1792  02151  170237          TDM     CLFLG
1793  02152  066225          BRGT    CLVER1
1794  02153  066156          BRGT    CLCOR1
1795  02154  170276          TDM     CLTC
1796  02155  066214          BRGT    CLPAUS
1797  02156  170160  CLCOR1  TDM     TEMP
1798  02157  046200          BRLE    CLCOR2
1799  02160  106256          LDX     SCCSUM
1800  02161  132162          STX     MCND
1801  02162  106074          LDX     THINCM
1802  02163  032143          BRS     MULT,3
1803         002345
1804  02165  132160          STX     TEMP
1805  02166  106226          LDX     FNLKTH
1806  02167  132162          STX     MCND
1807  02170  106073          LDX     DECAYM
1808  02171  032143          BRS     MULT,3
1809         002345
1810  02173  110160          ADD     TEMP
1811  02174  160075          CMP     CLTHMN
1812  02175  066177          BRGT    *+2
1813  02176  106075          LDX     CLTHMN
1814  02177  132226          STX     FNLKTH
1815  02200  170300  CLCOR2  TDM     VCLC
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1816  02201  046244          BRLE   CLTST1+2
1817  02202  170243          TDM    FRMLK
1818  02203  062343          BRGE   CLEXIT
1819  02204  170240          TDM    RCVEN
1820  02205  042207          BRLT   *+2
1821  02206  132240          STX    ENRCV
1822  02207  166231          STO    CLTRK
1823  02210  170272          TDM    RLTRK
1824  02211  062343          BRGE   CLEXIT
1825  02212  106152          LDX    MBIT10
1826  02213  072222          BR     CLVER1-3
1827  02214  164237  CLPAUS  STZ    CLFLG
1828  02215  106157          LDX    MBIT15
1829  02216  132256          STX    RCWMOD
1830  02217  106066          LDX    CLPCMX
1831  02220  132252          STX    CLPC
1832  02221  106143          LDX    MBIT3
1833  02222  116166          OR     LAMPS
1834  02223  132166          STX    LAMPS
1835  02224  072343          BR     CLEXIT
1836  02225  066343  CLVER1  BRGT   CLEXIT
1837  02226  170276          TDM    CLTC
1838  02227  066274          BRGT   CLTST3
1839  02230  166237          STO    CLFLG
1840  02231  170243          TDM    FRMLK
1841  02232  076234          BRNE   *+2
1842  02233  166242          STO    DPFLG
1843  02234  164252          STZ    CLPC
1844  02235  104141          LDC    MBIT1
1845  02236  120143          XOR    MBIT3
1846  02237  114166          AND    LAMPS
1847  02240  132166          STX    LAMPS
1848  02241  072244          BR     *+3
1849  02242  046251  CLTST1  BRLE   CLTST2
1850  02243  132237          STX    CLFLG
1851  02244  106067          LDX    VCLCMX
1852  02245  132300          STX    VCLC
1853  02246  106070          LDX    CLTCMN
1854  02247  132276          STX    CLTC
1855  02250  072343          BR     CLEXIT
1856  02251  106252  CLTST2  LDX    CLFSCH
1857  02252  042277          BRLT   CLTST4
1858  02253  017757          DEC    R
1859  02254  132252          STX    CLPC
1860  02255  066343          BRGT   CLEXIT
1861  02256  166252          STO    CLFSCH
1862  02257  104152          LDC    MBIT10
1863  02260  116266          OR     TXCLKF
1864  02261  114166          AND    LAMPS
1865  02262  116141          OR     MBIT1
1866  02263  132166          STX    LAMPS
1867  02264  164344          STZ    CADRI
1868  02265  164345          STZ    CADRI+1
1869  02266  164217          STZ    LKENBL
1870  02267  164240          STZ    RCVEN
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1871  02270  164231          STZ        CLTRK
1872  02271  164262          STZ        CLSCHI
1873  02272  106065          LDX        CLSCMX
1874  02273  132254          STX        CLSC
1875  02274  164256 CLTST3    STZ        RCWMOD
1876  02275  164257          STZ        CLFLG
1877  02276  072341          BR         CLEXIT-2
1878  02277  170254 CLTST4    TDM        CLSC
1879  02300  066312          BRGT       CLSRCH
1880  02301  170242          TDM        OPFLG
1881  02302  076317          BRNE       CLABT
1882  02303  010000          IOS        R
1883  02304  106201          LDX        RCNTR
1884  02305  011740          INC        R
1885  02306  132201          STX        RCNTR
1886  02307  006000          IEN        R
1887  02310  132242          STX        OPFLG
1888  02311  072271          BR         CLTST3-3
1889  02312  052143 CLSRCH    BRS        SEARCH,3
1890         001771
1891  02314  116156          OR         MBIT14
1892  02315  004012          OUT        '12
1893  02316  072343          BR         CLEXIT
1894  02317  170272 CLABT     TDM        RLTRK
1895  02320  056335          BREQ       REQSCH
1896  02321  170274          TDM        TXACQF
1897  02322  046325          BRLE       *+3
1898  02323  106117          LDX        CRDLY
1899  02324  072332          BR         STRDLY
1900  02325  170265          TDM        RLAQF
1901  02326  042331          BRLT       *+3
1902  02327  106120          LDX        FRDLY
1903  02330  072332          BR         STRDLY
1904  02331  106121          LDX        RLDLY
1905  02332  132374 STRDLY    STX        DLYC
1906  02333  132241          STX        RDRNGF
1907  02334  072340          BR         CLEXIT-3
1908  02335  106176 REQSCH    LDX        SWITCH
1909  02336  114034          AND        M'1700
1910  02337  132176          STX        SWITCH
1911  02340  164272          STZ        RLTRK
1912  02341  164275          STZ        RPTXED
1913  02342  164233          STZ        RNGLPF
1914  02343  032100 CLEXIT    BRP   (I)  CLRRTN
1915         003051
1916                *MULTIPLY SUBROUTINE
1917  02345  132163 MULT      STX        MPLR
1918  02346  012417          LDI        '17
1919  02347  164161          STZ        PROD
1920  02350  016600          CLC        R
1921  02351  102163          LDR        MPLR
1922  02352  132163          STX        MPLR
1923  02353  106162          LDX        MCND
1924  02354  126161          MPS        PROD
1925  02355  132161          STX        PROD
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1926  02356  176751          BRI     *-5
1927  02357  002043          SRT     3
1928                 *CORRECT TIMING SUBROUTINE
1929  02360  107256 CORR      LDX     SCCSUM,J
1930  02361  161124          CMP     SCGCBP,J
1931  02362  066364          BRGT    *+2
1932  02363  107124          LDX     SCGCBP,J
1933  02364  132162          STX     DEN
1934  02365  106157 TC/SM     LDX     MBIT15
1935  02366  132167          STX     SIGN
1936  02367  107260          LDX     SCCDIF,J
1937  02370  062374          BRGE    CORR0
1938  02371  164167          STZ     SIGN
1939  02372  001760          CMX     R
1940  02373  011740          INC     R
1941  02374  160162 CORR0     CMP     DEN
1942  02375  002100          BRPLT (I) CORR1
1943         002401
1944  02377  107122          LDX     CLGF,J
1945  02400  072022          BR      CORR2
1946  02401  132163 CORR1     STX     NUM
1947  02402  012417          LDI     15
1948  02403  164173          STZ     TEMP5
1949  02404  016600          CLC     R
1950  02405  130162          DVS     DEN
1951  02406  132163          STX     NUM
1952  02407  100173          LDL     TEMP5
1953  02410  132173          STX     TEMP5
1954  02411  100163          LDL     NUM
1955  02412  176405          BRI     *-5
1956  02413  107122          LDX     CLGF,J
1957  02414  132162          STX     MCND
1958  02415  100173          LDL     TEMP5
1959  02416  032143          BRS     MULT,3
1960         002345
1961  02420  070022          BRNC    CORR2
1962  02421  011740          INC     R
1963  02422  116167 CORR2     OR      SIGN
1964  02423  114376          AND     ENCORR
1965  02424  133250          STX     CLCORR,J
1966  02425  015000          TJX     R
1967  02426  036042          SRTNE   2
1968  02427  106156          LDX     MBIT14
1969  02430  116250          OR      CLCORR
1970  02431  004012          OUT     *12
1971  02432  032042 CORREX    SRT     2
1972                 *RANGE LOOP ROUTINE
1973  02433  164253 RLROUT    STZ     RNGLPF
1974  02434  015001          LDJ     1
1975  02435  106256          LDX     SCCSUM
1976  02436  132162          STX     MCND
1977  02437  106107          LDX     SRLTPM
1978  02440  032143          BRS     MULT,3
1979         002345
1980  02442  112257          SUB     RSUM
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1981  02443  132160          STX     TEMP
1982  02444  002142          BRSLT   CORR,2
1983         002360
1984  02446  106160          LDX     TEMP
1985  02447  170273          TDM     RLFLG
1986  02450  056103          BREQ    RLTST1
1987  02451  062055          BRGE    *+4
1988  02452  106277          LDX     RLTC
1989  02453  017757          DEC     R
1990  02454  132277          STX     RLTC
1991  02455  106301          LDX     VRLC
1992  02456  017757          DEC     R
1993  02457  132301          STX     VRLC
1994  02460  066175          BRGT    RLEXIT
1995  02461  106277          LDX     RLTC
1996  02462  170273          TDM     RLFLG
1997  02463  066072          BRGT    RLVER1
1998  02464  046106          BRLE    RLTST1+3
1999  02465  106104  RLPAS1   LDX     RLPCMX
2000  02466  132253          STX     RLPC
2001  02467  106166          LDX     LAMPS
2002  02470  116151          OR      MBIT9
2003  02471  072173          BR      RLEXIT-2
2004  02472  066174  RLVER1   BRGT    RLEXIT-1
2005  02473  166272          STO     RLTRK
2006  02474  166265          STO     RLAQF
2007  02475  166273          STO     RLFLG
2008  02476  164263          STZ     RLSCHI
2009  02477  106005          LDX     M*17
2010  02500  114166          AND     LAMPS
2011  02501  132166          STX     LAMPS
2012  02502  072106          BR      RLTST1+3
2013  02503  062113  RLTST1   BRGE    RLTST2
2014  02504  106140          LDX     MBIT0
2015  02505  132273          STX     RLFLG
2016  02506  106105          LDX     VRLCMX
2017  02507  132301          STX     VRLC
2018  02510  106106          LDX     RLTCMN
2019  02511  132277          STX     RLTC
2020  02512  072175          BR      RLEXIT
2021  02513  106253  RLTST2   LDX     RLFSCH
2022  02514  046127          BRLE    RLSCH
2023  02515  017757          DEC     R
2024  02516  132253          STX     RLPC
2025  02517  066175          BRGT    RLEXIT
2026  02520  106103          LDX     RLSCMX
2027  02521  132255          STX     RLSC
2028  02522  132272          STX     RLTRK
2029  02523  104152          LDC     MBIT10
2030  02524  114166          AND     LAMPS
2031  02525  116147          OR      MBIT7
2032  02526  072173          BR      RLEXIT-2
2033  02527  106265  RLSCH    LDX     RLAQF
2034  02530  017757          DEC     R
2035  02531  066162          BRGT    RLSCH1
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2036  02532  170255          TDM       RLSC
2037  02533  046137          BRLE      *+4
2038  02534  032143          BRS       SEARCH,3
2039         001771
2040  02536  072165          BR        RLABT-2
2041  02537  170265          TDM       RLAQF
2042  02540  042167          BRLT      RLABT
2043  02541  106264          LDX       RAQC
2044  02542  042167          BRLT      RLABT
2045  02543  160102          CMP       RAQCMX
2046  02544  042151          BRLT      *+5
2047  02545  166264          STO       RAQC
2048  02546  017737          RS        R
2049  02547  132265          STX       RLAQF
2050  02550  072156          BR        *+6
2051  02551  011740          INC       R
2052  02552  132265          STX       RLAQF
2053  02553  132264          STX       RAQC
2054  02554  106103          LDX       RLSCMX
2055  02555  132255          STX       RLSC
2056  02556  106313          LDX       JMPSGN
2057  02557  120157          XOR       MBIT15
2058  02560  132313          STX       JMPSGN
2059  02561  072164          BR        *+3
2060  02562  132265  RLSCH1   STX       RLAQF
2061  02563  106313          LDX       JMPSGN
2062  02564  116112          OR        JMPINC
2063  02565  132251          STX       RLCORR
2064  02566  072175          BR        RLEXIT
2065  02567  164272  RLABT    STZ       RLTRK
2066  02570  104005          LDC       M'17
2067  02571  116166          OR        LAMPS
2068  02572  120152          XOR       MBIT10
2069  02573  132166          STX       LAMPS
2070  02574  164273          STZ       RLFLG
2071  02575  032100  RLEXIT   BRP  (I)  RLRRTN
2072         003054
2073                *INITIALIZE TRANSMIT TIMING ROUTINE
2074  02577  132261  INITRL    STX       RLINIT
2075  02600  104022          LDC       M'60
2076  02601  114176          AND       SWITCH
2077  02602  132176          STX       SWITCH
2078  02603  106140          LDX       MBIT0
2079  02604  132272          STX       RLTRK
2080  02605  164275          STZ       RPTXED
2081  02606  164374          STZ       DLYC
2082  02607  166241          STO       RDRNGF
2083  02610  106261          LDX       RLINIT
2084  02611  066223          BRGT      RLIN1
2085  02612  170274          TDM       TXACQF
2086  02613  046255          BRLE      RLIN3
2087  02614  106113          LDX       CRSINC
2088  02615  120157          XOR       MBIT15
2089  02616  132251          STX       RLCORR
2090  02617  106211          LDX       RANGE2
```

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2091  02620  132177          STX     ITEMP
2092  02621  106210          LDX     RANGE1
2093  02622  072244          BR      RLIN2
2094  02623  164265  RLIN1   STZ     RLAQF
2095  02624  162144          TST     MBIT4
2096  02625  056266          BREQ    RLIN4
2097  02626  170004          TOM     FMT
2098  02627  042322          BRLT    RLINEX
2099  02630  106114          LDX     CRSCMX
2100  02631  132257          STX     CRSC
2101  02632  132274          STX     TXACQF
2102  02633  164277          STZ     CRTC
2103  02634  164301          STZ     CRPC
2104  02635  011242          INP     2
2105  02636  162142          TST     MBIT2
2106  02637  056242          BREQ    *+3
2107  02640  106057          LDX     RTSD2
2108  02641  072243          BR      *+2
2109  02642  106056          LDX     RTSD1
2110  02643  164177          STZ     ITEMP
2111  02644  032141  RLIN2   BRS     INITTX.1
2112         001372
2113  02646  104005          LDC     M'17
2114  02647  116166          OR      LAMPS
2115  02650  120144          XOR     MBIT4
2116  02651  120152          XOR     MBIT10
2117  02652  132166          STX     LAMPS
2118  02653  166261          STO     RLINIT
2119  02654  072206          BR      RLIN4
2120  02655  106263  RLIN3   LDX     RLSCHI
2121  02656  120157          XOR     MBIT15
2122  02657  017757          RS      R
2123  02660  162156          TST     MBIT14
2124  02661  056263          BREQ    *+2
2125  02662  120053          XOR     C37777
2126  02663  132251          STX     RLCORR
2127  02664  170265          TOM     RLAQF
2128  02665  062270          BRGE    RLIN5-3
2129  02666  164264  RLIN4   STZ     RAQC
2130  02667  164313          STZ     JMPSGN
2131  02670  106103          LDX     RLSCMX
2132  02671  132255          STX     RLSC
2133  02672  164263          STZ     RLSCHI
2134  02673  164253  RLIN5   STZ     RLFSCH
2135  02674  164273          STZ     RLFLG
2136  02675  170261          TOM     RLINIT
2137  02676  042322          BRLT    RLINEX
2138  02677  106166          LDX     LAMPS
2139  02700  114005          AND     M'17
2140  02701  116023          OR      M'600
2141  02702  132166          STX     LAMPS
2142  02703  170261          TOM     RLINIT
2143  02704  056310          BREQ    RLIN6
2144  02705  011242          INP     2
2145  02706  162142          TST     MBIT2
```

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2146  02707  056314                BREQ        RLIN7
2147  02710  106211  RLIN6         LDX         RANGE2
2148  02711  132177                STX         ITEMP
2149  02712  106210                LDX         RANGE1
2150  02713  072317                BR          RLIN8
2151  02714  106061  RLIN7         LDX         IRNG2
2152  02715  132177                STX         ITEMP
2153  02716  106060                LDX         IRNG1
2154  02717  032141  RLIN8         BRS         INITTX,1
2155         001372
2156  02721  166274                STO         TXACQF
2157  02722  032100  RLINEX        BRP   (I)   RSIE)
2158         001350
2159                  *INITIALIZE ROUTINE
2160  02724  012417  INIT          LDI         15
2161  02725  001763                CLX         R
2162  02726  004012                OUT         *12
2163  02727  004014                OUT         *14
2164  02730  004015                OUT         *15
2165  02731  010600                SOC         R
2166  02732  013707                RSC         R
2167  02733  132540                STX         MBIT0,I
2168  02734  176732                BRI         *-2
2169  02735  011243                INP         3
2170  02736  114024                AND         M*6000
2171  02737  132135                STX         NCTSLT
2172  02740  132136                STX         NCTIO
2173  02741  011243                INP         3
2174  02742  162134                TST         MBIT12
2175  02743  076361                BRNE        HRF
2176  02744  164004  LRF           STZ         FMT
2177  02745  102135                LDR         NCTSLT
2178  02746  017707                RS          R
2179  02747  017707                RS          R
2180  02750  132135                STX         NCTSLT
2181  02751  013404                LDK         4
2182  02752  011243                INP         3
2183  02753  017737                RS          R
2184  02754  017677                LS          R
2185  02755  177754                BRK         *-1
2186  02756  114044                AND         MFMT
2187  02757  132143                STX         CRADR
2188  02760  072375                BR          INIT1
2189  02761  166004  HRF           STO         FMT
2190  02762  106017                LDX         M*7777
2191  02763  132044                STX         MFMT
2192  02764  104006                LDC         M*177
2193  02765  132045                STX         MTADR
2194  02766  106007                LDX         M*1777
2195  02767  132046                STX         MNCTID
2196  02770  132047                STX         MRANGE
2197  02771  106140                LDX         MBITO
2198  02772  132052                STX         SOFCW
2199  02773  106051                LDX         RORNGH
2200  02774  132050                STX         RORNG
```

```
2201   02775   011243   INIT1    INP        3
2202   02776   017677            LS         R
2203   02777   017677            LS         R
2204   03000   114030            AND        C'17
2205   03001   132160            STX        TEMP
2206   03002   011243            INP        3
2207   03003   114010            AND        M'3
2208   03004   116160            OR         TEMP
2209   03005   017677            LS         R
2210   03006   114044            AND        MFMT
2211   03007   132134            STX        LRADR
2212   03010   013406            LDK        6
2213   03011   011243            INP        3
2214   03012   017677            LS         R
2215   03013   177412            BRK        *-1
2216   03014   114045            AND        MTADR
2217   03015   132137            STX        TADR
2218   03016   106110   CLRBS    LDX        BSADR1
2219   03017   132160            STX        DMADR
2220   03020   106012            LDX        M'377
2221   03021   032143            BRS        STZBS,3
2222           001361
2223   03023   013402            LDK        2
2224   03024   106020            LDX        M'30
2225   03025   133564            STX        DLAMPS,K
2226   03026   177425            BRK        *-1
2227   03027   106007            LDX        M'1777
2228   03030   132166            STX        LAMPS
2229   03031   004017            OUT        '17
2230   03032   166376            STO        ENCORR
2231   03033   006000            IEN        R
2232   03034   170235   RUN      TDM        CLINIT
2233   03035   056043            BREQ       *+6
2234   03036   106111   INITCL   LDX        BSADR2
2235   03037   132160            STX        DMADR
2236   03040   106126            LDX        BSADR3
2237   03041   032143            BRS        STZBS,3
2238           001361
2239   03043   170232            TDM        CLKLPF
2240   03044   056051            BREQ       CLRRTN
2241   03045   106202            LDX        RSLOT
2242   03046   160014            CMP        M'7
2243   03047   026100            BRPGT (I)  CLROUT
2244           002010
2245   03051   170233   CLRRTN   TDM        RNGLPF
2246   03052   036100            BRPNE (I)  RLROUT
2247           002433
2248   03054   170234   RLRRTN   TDM        LINKF
2249   03055   026100            BRPGT (I)  LKROUT
2250           003404
2251   03057   106202   LKRRTN   LDX        RSLOT
2252   03060   160035            CMP        C24
2253   03061   066034            BRGT       RUN
2254   03062   112144            SUB        MBIT4
2255   03063   114231            AND        CLTRK
```

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2256  03064  046034            BRLE    RUN
2257                  *DEVICE-SWITCH SERVICE ROUTINE
2258  03065  106221  SWROUT    LDX     SWPNTR
2259  03066  011740            INC     R
2260  03067  114140            AND     MBIT0
2261  03070  132221            STX     SWPNTR
2262  03071  002400            TXI     R
2263  03072  010000            IOS     F
2264  03073  004007            OUT     7
2265  03074  011247            INP     7
2266  03075  114030            AND     C'17
2267  03076  132160            STX     TEMP
2268  03077  011251            INP     '11
2269  03100  006000            IEN     R
2270  03101  132163            STX     TEMP3
2271  03102  114031            AND     C'3777
2272  03103  132161            STX     TEMP1
2273  03104  114155            AND     MBIT13
2274  03105  132167            STX     TEMP4
2275  03106  106025            LDX     M'7000
2276  03107  114163            AND     TEMP3
2277  03110  132163            STX     TEMP3
2278  03111  106266            LDX     TXCLKF
2279  03112  116265            OR      RLAQF
2280  03113  132173            STX     TEMP5
2281  03114  104025            LDC     M'7000
2282  03115  114574            AND     DSWTCH,I
2283  03116  116163            OR      TEMP3
2284  03117  132574            STX     DSWTCH,I
2285  03120  162151            TST     MBIT9
2286  03121  056127            BREQ    *+6
2287  03122  114151            AND     MBIT9
2288  03123  164564            STZ     DLAMPS,I
```

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2289  03124  032142          BRS     TERMLK+6,2
2290         000144
2291  03126  072351          BR      SWEXIT
2292  03127  170704          TDM     AKLKWD,I
2293  03130  056133          BREG    *+3
2294  03131  170173          TDM     TEMP5
2295  03132  042140          BRLT    SWCONT
2296  03133  170740          TDM     BADRT,I
2297  03134  076175          BRNE    TSTBMP
2298  03135  162152          TST     MBIT10
2299  03136  056175          BREG    TSTBMP
2300  03137  042206          BRLT    LOCALL
2301  03140  013003  SWCONT  LDJ     3
2302  03141  162142          TST     MBIT2
2303  03142  076213          BRNE    LCLCNT
2304  03143  162141          TST     MBIT1
2305  03144  076230          BRNE    RELASG
2306  03145  170173          TDM     TEMP5
2307  03146  062155          BRGE    CLRLNK-2
2308  03147  170750          TDM     TLKWD1,I
2309  03150  076351          BRNE    SWEXIT
2310  03151  162140          TST     MBIT0
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2311  03152  076300          BRNE    REQASG
2312  03153  162143          TST     MBIT3
2313  03154  076327          BRNE    REQLNK
2314  03155  162144          TST     MBIT4
2315  03156  056351          BREQ    SWEXIT
2316  03157  116143  CLRLNK  OR      MBIT3
2317  03160  120020          XOR     M'30
2318  03161  132574          STX     DSWTCH,I
2319  03162  162156          TST     MBIT14
2320  03163  056166          BREQ    *+3
2321  03164  106740          LDX     BADRT,I
2322  03165  072170          BR      *+3
2323  03166  106160          LDX     TEMP
2324  03167  116141          OR      MBIT1
2325  03170  116142          OR      MBIT2
2326  03171  132750          STX     TLKWD1,I
2327  03172  032142          BRS     TERMLK,2
2328                 000136
2329  03174  072351          BR      SWEXIT
2330  03175  162145  TSTBMP  TST     MBIT5
2331  03176  056140          BREQ    SWCONT
2332  03177  120145          XOR     MBIT5
2333  03200  132574          STX     DSWTCH,I
2334  03201  106742          LDX     WADRT,I
2335  03202  116142          OR      MBIT2
2336  03203  116143          OR      MBIT3
2337  03204  132704          STX     AKLKWD,I
2338  03205  072351          BR      SWEXIT
2339  03206  106742  LDCALL  LDX     WADRT,I
2340  03207  164742          STZ     WADRT,I
2341  03210  032143          BRS     ENCALL,3
2342                 000176
2343  03212  072351          BR      SWEXIT
2344  03213  120142  LCLCNT  XOR     MBIT2
2345  03214  162054          TST     M'1700
2346  03215  076350          BRNE    SWEXIT-1
2347  03216  116150          OR      MBIT8
2348  03217  132574          STX     DSWTCH,I
2349  03220  106160          LDX     TEMP
2350  03221  017737          RS      R
2351  03222  177221          BRJ     *-1
2352  03223  116161          OR      TEMP1
2353  03224  116140          OR      MBIT0
2354  03225  032142          BRS     ENASG?,2
2355                 000155
2356  03227  072351          BR      SWEXIT
2357  03230  162143  RELASG  TST     MBIT3
2358  03231  076276          BRNE    CLRREL
2359  03232  162150          TST     MBIT8
2360  03233  056255          BREQ    NOTLCL
2361  03234  102564          LDR     DLAMPS,I
2362  03235  070250          BRNC    LCLASG
2363  03236  170173          TDM     TEMP5
2364  03237  062250          BRGE    LCLASG
2365  03240  170750          TDM     TLKWD1,I
```

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2366  03241  076351          BRNE    SWEXIT
2367  03242  017677          LS      R
2368  03243  132564          STX     DLAMPS,I
2369  03244  106706          LDX     RINNCT,I
2370  03245  132750          STX     TLKWD1,I
2371  03246  106574          LDX     DSWTCH,I
2372  03247  072276          BR      CLRREL
2373  03250  106574  LCLASG  LDX     DSWTCH,I
2374  03251  162155          TST     MBIT13
2375  03252  076276          BRNE    CLRREL
2376  03253  106564          LDX     DLAMPS,I
2377  03254  072267          BR      RELCOM
2378  03255  162155  NOTLCL  TST     MBIT13
2379  03256  076276          BRNE    CLRREL
2380  03257  170173          TDM     TEMP5
2381  03260  062253          BRGE    NOTLCL-2
2382  03261  170750          TDM     TLKWD1,I
2383  03262  076351          BRNE    SWEXIT
2384  03263  106706          LDX     RINNCT,I
2385  03264  132750          STX     TLKWD1,I
2386  03265  104140          LDC     MBIT0
2387  03266  114564          AND     DLAMPS,I
2388  03267  114011  RELCOM  AND     M'37
2389  03270  116143          OR      MBIT3
2390  03271  132564          STX     DLAMPS,I
2391  03272  164772          STZ     RCVCW,I
2392  03273  164770          STZ     TXCW,I
2393  03274  104064          LDC     M'1700
2394  03275  114574          AND     DSWTCH,I
2395  03276  120141  CLRREL  XOR     MBIT1
2396  03277  072350          BR      SWEXIT-1
2397  03300  120140  REQASG  XOR     MBIT0
2398  03301  132574          STX     DSWTCH,I
2399  03302  162023          TST     MASG
2400  03303  076351          BRNE    SWEXIT
2401  03304  162146          TST     MBIT6
2402  03305  076324          BRNE    REQAS1
2403  03306  116146          OR      MBIT6
2404  03307  132574          STX     DSWTCH,I
2405  03310  014400          TIX     R
2406  03311  011740          INC     R
2407  03312  017677          LS      R
2408  03313  177312          BRJ     *-1
2409  03314  116161          OR      TEMP1
2410  03315  162153          TST     MBIT11
2411  03316  056321          BREQ    *+3
2412  03317  120153          XOR     MBIT11
2413  03320  116143          OR      MBIT3
2414  03321  116136          OR      NCTID
2415  03322  116151          OR      MBIT9
2416  03323  132706          STX     RTNNCT,I
2417  03324  106706  REQAS1  LDX     RINNCT,I
2418  03325  116142          OR      MBIT2
2419  03326  072346          BR      SWEXIT-3
2420  03327  120143  REQLNK  XOR     MBIT3
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AD-A035 479 OHIO STATE UNIV COLUMBUS ELECTROSCIENCE LAB F/G 17/2
A MODEM/CONTROLLER FOR TDMA COMMUNICATIONS SYSTEMS.(U)
DEC 76 R C TAYLOR, R J HUFF F30602-72-C-0162
UNCLASSIFIED ESL-3364-5 RADC-TR-76-362 NL

2 OF 2
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END

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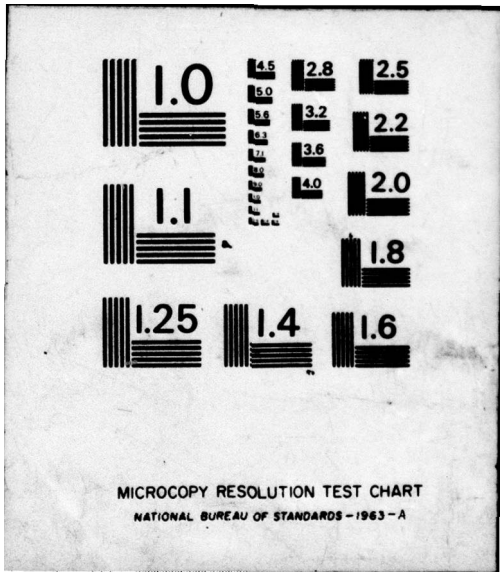
1.0
1.1
1.25
1.4
1.6
1.8
2.0
2.2
2.5
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3.2
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MICROCOPY RESOLUTION TEST CHART
NATIONAL BUREAU OF STANDARDS - 1963 - A

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2421  03330  162023            TST       MASG
2422  03331  056350            BREQ      SWEXIT-1
2423  03332  162156            TST       MBIT14
2424  03333  076350            BRNE      SWEXIT-1
2425  03334  116155            OR        MBIT13
2426  03335  032142            BRS       TERMEX-5,2
2427         000167
2428  03337  104155            LDC       MBIT13
2429  03340  114756            AND       ASMT,1
2430  03341  116167            OR        TEMP4
2431  03342  132752            STX       TLKWD2,I
2432  03343  106160            LDX       TEMP
2433  03344  116141            OR        MBIT1
2434  03345  132740            STX       BADRT,I
2435  03346  132750            STX       TLKWD1,I
2436  03347  072351            BR        *+2
2437  03350  132574            STX       DSWTCH,I
2438  03351  072034  SWEXIT    BR        RUN
2439                 *LINK WORD VERIFICATION SUBROUTINE
2440  03352  106714  TST2/3    LDX       NRLKWD,I
2441  03353  161320            CMP       LRLKWD,J
2442  03354  056365            BREQ      T2/3EX
2443  03355  161330            CMP       ORLKWD,J
2444  03356  056365            BREQ      T2/3EX
2445  03357  107320            LDX       LRLKWD,J
2446  03360  133330            STX       ORLKWD,J
2447  03361  106714            LDX       NRLKWD,I
2448  03362  133320            STX       LRLKWD,J
2449  03363  001763            CLX       R
2450  03364  072367            BR        T2/3EX+2
2451  03365  165320  T2/3EX    STZ       LRLKWD,J
2452  03366  165330            STZ       ORLKWD,J
2453  03367  132160            STX       TEMP
2454  03370  042043            SRT       3
2455                 *SUBROUTINE FOR RIGHT-SHIFTING TERMINAL
2456  03371  012403  RSADR     LDI       3          ADDRESS
2457  03372  017757            RS        R
2458  03373  176772            BRI       *-1
2459  03374  114014            AND       M'7
2460  03375  017757            DEC       R
2461  03376  042057            BRLT      LKRRTN
2462  03377  160140            CMP       MBIT0
2463  03400  066374            BRGT      LKEXIT
2464  03401  002400            TXI       R
2465  03402  106161            LDX       TEMP1
2466  03403  032043            SRT       3
2467                 *LINK ROUTINE
2468  03404  106230  LKROUT    LDX       LWCNTR
2469  03405  017757            DEC       R
2470  03406  132230            STX       LWCNTR
2471  03407  002400            TXI       R
2472  03410  066016            BRGT      LINK0
2473  03411  166264            STO       LINKF
2474  03412  106310            LDX       LSADR
2475  03413  056374            BREQ      LKEXIT
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2476  03414  001760          CMX     R
2477  03415  056302          BREQ    NCTLNK
2478  03416  013005  LINK0   LDJ     5
2479  03417  104006          LDC     M'177
2480  03420  115340          AND     BADRT,J
2481  03421  160710          CMP     LSADR,I
2482  03422  076111          BRNE    LINK5
2483  03423  032143          BRS     TST2/3,3
2484         003352
2485  03425  015000          TJX     R
2486  03426  160142          CMP     MBIT2
2487  03427  062147          BRGE    VCALL?
2488  03430  106160          LDX     TEMP
2489  03431  120137          XOR     TADR
2490  03432  162045          TST     MTADR
2491  03433  076111          BRNE    LINK5
2492  03434  121340          XOR     BADRT,J
2493  03435  162026          TST     MDEV
2494  03436  076111          BRNE    LINK5
2495  03437  114005          AND     M'17
2496  03440  056111          BREQ    LINK5
2497  03441  114010          AND     M'3
2498  03442  076111          BRNE    LINK5
2499  03443  015000          TJX     R
2500  03444  002400          TXI     R
2501  03445  160140          CMP     MBIT0
2502  03446  046070          BRLE    LINK1
2503  03447  114140          AND     MBIT0
2504  03450  002400          TXI     R
2505  03451  106160          LDX     TEMP
2506  03452  162143          TST     MBIT3
2507  03453  076107          BRNE    LINK4
2508  03454  106742          LDX     WADRT,I
2509  03455  160740          CMP     BADR1,I
2510  03456  076061          BRNE    *+3
2511  03457  164720          STZ     LRLKWD,I
2512  03460  164730          STZ     ORLKWD,I
2513  03461  164742          STZ     WADRT,I
2514  03462  104014          LDC     M'7
2515  03463  116140          OR      MBIT0
2516  03464  114564          AND     DLAMPS,I
2517  03465  132564          STX     DLAMPS,I
2518  03466  104157          LDC     MBIT15
2519  03467  072141          BR      LINK6
2520  03470  106160  LINK1   LDX     TEMP
2521  03471  162143          TST     MBIT3
2522  03472  076076          BRNE    LINK2
2523  03473  032142          BRS     TERMLK,2
2524         000136
2525  03475  072374          BR      LKEXIT
2526  03476  162142  LINK2   TST     MBIT2
2527  03477  056103          BREQ    LINK3
2528  03500  106005          LDX     M'17
2529  03501  114564          AND     DLAMPS,I
2530  03502  072373          BR      LKEXIT-1
```

```
2531  03503  104144  LINK3   LDC     MBIT4
2532  03504  114564          AND     DLAMPS,I
2533  03505  116145          OR      MBIT5
2534  03506  072373          BR      LKEXIT-1
2535  03507  106230  LINK4   LDX     L.CNTR
2536  03510  002400          TXI     R
2537  03511  177017  LINK5   BRJ     LINK0+1
2538  03512  106045          LDX     MTADR
2539  03513  116005          OR      M.17
2540  03514  114714          AND     NRLKWD,I
2541  03515  120141          XOR     MBIT1
2542  03516  160137          CMP     TADR
2543  03517  076374          BRNE    LKEXIT
2544  03520  106714          LDX     NRLKWD,I
2545  03521  132161          STX     TEMP1
2546  03522  114026          AND     MDEV
2547  03523  116710          OR      LSADR,I
2548  03524  116141          OR      MBIT1
2549  03525  132160          STX     TEMP
2550  03526  032143          BRS     RSADR,3
2551         003371
2552  03530  170744          TOW     CADR1,I
2553  03531  076374          BRNE    LKEXIT
2554  03532  132724          STX     LCLKWD,I
2555  03533  164734          STZ     OCLKWD,I
2556  03534  106160          LDX     TEMP
2557  03535  132744          STX     CADRT,I
2558  03536  106141          LDX     MBIT1
2559  03537  132746          STX     CPNTR,I
2560  03540  104154          LDC     MBIT12
2561  03541  114574  LINK6   AND     DSWTCH,I
2562  03542  132574          STX     DSWTCH,I
2563  03543  162151          TST     MBIT9
2564  03544  056374          BREQ    LKEXIT
2565  03545  164744  LINKEX  STZ     CADR1,I
2566  03546  072374          BR      LKEXIT
2567  03547  114140  VCALL?   AND     MBIT0
2568  03550  002400          TXI     R
2569  03551  106160          LDX     TEMP
2570  03552  076164          BRNE    VCALL2
2571  03553  106746          LDX     CPNTR,I
2572  03554  017757          DEC     R
2573  03555  132746          STX     CPNTR,I
2574  03556  076107          BRNE    LINK4
2575  03557  164744  VCALL1  STZ     CADRT,I
2576  03560  104154          LDC     MBIT12
2577  03561  114574          AND     DSWTCH,I
2578  03562  132574          STX     DSWTCH,I
2579  03563  072107          BR      LINK4
2580  03564  120141  VCALL2  XOR     MBIT1
2581  03565  162005          TST     M.17
2582  03566  076177          BRNE    VCALL3
2583  03567  114045          AND     MTADR
2584  03570  160137          CMP     TADR
2585  03571  076157          BRNE    VCALL1
```

```
2586  03572  106142          LDX     MBIT2
2587  03573  132746          STX     CPNTR,I
2588  03574  106574          LDX     DSWTCH,I
2589  03575  116154          OR      MBIT12
2590  03576  072162          BR      VCALL1+3
2591  03577  162140  VCALL3   TST     MBIT0
2592  03600  056157          BREQ    VCALL1
2593  03601  106574          LDX     DSWTCH,I
2594  03602  162154          TST     MBIT12
2595  03603  056157          BREQ    VCALL1
2596  03604  120154          XOR     MBIT12
2597  03605  132574          STX     DSWTCH,I
2598  03606  120160          XOR     TEMP
2599  03607  114153          AND     MBIT11
2600  03610  076157          BRNE    VCALL1
2601  03611  170704          TDM     AKLKWD,I
2602  03612  056215          BREQ    *+3
2603  03613  170271          TDM     TXEN
2604  03614  042145          BRLT    LINKEX
2605  03615  106574          LDX     DSWTCH,I
2606  03616  162156          TST     MBIT14
2607  03617  056227          BREQ    *+8
2608  03620  106744          LDX     CADRT,I
2609  03621  160740          CMP     BADRT,I
2610  03622  076226          BRNE    *+4
2611  03623  116143          OR      MBIT3
2612  03624  132704          STX     AKLKWD,I
2613  03625  072145          BR      LINKEX
2614  03626  106574          LDX     DSWTCH,I
2615  03627  042262          BRLT    VCALL7
2616  03630  162052          TST     C17777
2617  03631  076242          BRNE    VCALL4
2618  03632  162152          TST     MBIT10
2619  03633  056242          BREQ    VCALL4
2620  03634  106160          LDX     TEMP
2621  03635  132754          STX     NXTASG,I
2622  03636  106744          LDX     CADRT,I
2623  03637  032143          BRS     ENCALL,3
2624         000176
2625  03641  072145          BR      LINKEX
2626  03642  116157  VCALL4   OR      MBIT15
2627  03643  132574          STX     DSWTCH,I
2628  03644  106744          LDX     CADRT,I
2629  03645  116143          OR      MBIT3
2630  03646  116142  VCALL5   OR      MBIT2
2631  03647  132704          STX     AKLKWD,I
2632  03650  106744          LDX     CADRT,I
2633  03651  132742          STX     WADRT,I
2634  03652  106160          LDX     TEMP
2635  03653  132754          STX     NXTASG,I
2636  03654  162155          TST     MBIT13
2637  03655  056276          BREQ    VCALL8
2638  03656  104141          LDC     MBIT1
2639  03657  114564  VCALL6   AND     DLAMPS,I
2640  03660  116142          OR      MBIT2
```

```
2641  03661  072300                BR        VCALL6+2
2642  03662  106744  VCALL7        LDX       CADRT,I
2643  03663  160742                CMP       WADRT,I
2644  03664  056245                BREQ      VCALL5-1
2645  03665  104160                LDC       TEMP
2646  03666  116754                OR        NXTASG,I
2647  03667  162155                TST       MBIT13
2648  03670  076145                BRNE      LINKEX
2649  03671  106574                LDX       DSWTCH,I
2650  03672  116145                OR        MBIT5
2651  03673  132574                STX       DSWTCH,I
2652  03674  106742                LDX       WADRT,I
2653  03675  072246                BR        VCALL5
2654  03676  106141  VCALL8        LDX       MBIT1
2655  03677  116564                OR        DLAMPS,I
2656  03700  132564                STX       DLAMPS,I
2657  03701  072145                BR        LINKEX
2658                 *NETWORK CONTROL TERMINAL LINK ROUTINE
2659  03702  013006  NCTLNK        LDJ       6
2660  03703  032143                BRS       TST2/3,3
2661                 003352
2662  03705  013007                LDJ       7
2663  03706  012403                LDI       3
2664  03707  016143                BRSEQ     TST2/3+5,3
2665                 003357
2666  03711  056374                BREQ      LKEXIT
2667  03712  132161                STX       TEMP1
2668  03713  114045                AND       MTADR
2669  03714  160137                CMP       TADR
2670  03715  076374                BRNE      LKEXIT
2671  03716  032143                BRS       TST2/3,3
2672                 003352
2673  03720  056374                BREQ      LKEXIT
2674  03721  106161                LDX       TEMP1
2675  03722  032143                BRS       RSADR,3
2676                 003371
2677  03724  162143                TST       MBIT3
2678  03725  056371                BREQ      NCTLK4
2679  03726  106574  NCTLK1        LDX       DSWTCH,I
2680  03727  162146                TST       MBIT6
2681  03730  056374                BREQ      LKEXIT
2682  03731  106002                LDX       C17777
2683  03732  114706                AND       RTNNCI,I
2684  03733  132163                STX       TEMP3
2685  03734  100160                LDL       TEMP
2686  03735  132162                STX       TEMP2
2687  03736  017677                LS        R
2688  03737  114154                AND       MBIT12
2689  03740  116163                OR        TEMP3
2690  03741  132163                STX       TEMP3
2691  03742  120706                XOR       RTNNCI,I
2692  03743  162154                TST       MBIT12
2693  03744  076374                BRNE      LKEXIT
2694  03745  162143                TST       MBIT3
2695  03746  056352                BREQ      NCTLK2
```

```
2696  03747  106163           LDX        TEMP3
2697  03750  116153           OR         MBIT11
2698  03751  132163           STX        TEMP3
2699  03752  170004  NCTLK2   TDM        FMT
2700  03753  042360           BRLT       NCTLK3
2701  03754  106706           LDX        RINNC1,I
2702  03755  120161           XOP        TEMP1
2703  03756  114033           AND        C37777
2704  03757  076374           BRNE       LKEXIT
2705  03760  106574  NCTLK3   LDX        DSWTCH,I
2706  03761  120021           XOR        M'30C
2707  03762  132574           STX        DSWTCH,I
2708  03763  106162           LDX        TEMP2
2709  03764  114013           AND        M'3777
2710  03765  116163           OR         TEMP3
2711  03766  032142           BRS        ENASG?,2
2712         000155
2713  03770  072374           BR         LKEXIT
2714  03771  106564  NCTLK4   LDX        DLAMPS,I
2715  03772  116140           OR         MBIT0
2716  03773  132564           STX        DLAMPS,I
2717  03774  032100  LKEXIT   BRP   (I)  LKRRTN
2718         003057
```

APPENDIX III
RANDOM-ACCESS MEMORY LOADING PROCEDURES

A. Corrections

For modems equipped with RAM type memory, the contents of control memory must be loaded into the modem from an external source each time the modem is turned on. An external computer jack located on the rear panel of the modem is used to do this. The 18 connections needed are shown in drawing 301. The connections are labeled as follows. (See drawing 301 for the correct pin numbers.)

GND	- ground
CNTRL	- the control line
ECOB00-ECOB15	- the data lines with ECOB00 being the low order bit.

The remaining connections are used when the modem is configured as a network controller and are used for passing information to a network program developed by the computer sciences corporation. They are not used in this application.

B. Loading Procedures

The use of the above lines along with the three switches found on the rear panel of the modem allow the contents of control memory to be loaded as follows:

1) move the LPC/LCM switch to LPC and the WE/WP switch to WE;
2) halt the computer by moving the Start/Halt switch to halt;
3) the modem computer is now ready to load its program counter with the first (lowest) memory location to be loaded. (This will normally be location 0) Placing the binary value of the first location on the bus and providing a positive strobe pulse to the control line causes this value to be loaded into the program counter.
4) the computer is now ready to accept memory contents, to enable this move the LPC/LCM switch to LCM.
5) consecutive memory locations are now loaded by placing the contents on the external computer data bus and strobing the control line. There is no minimum clocking rate, and rates as high as 2 MHz can be used providing the data is stable on the bus when the control line is strobed.
6) when all the desired locations have been loaded, the memory is protected by moving the WE/WP switch to WP.

C. Programs for Loading Control Memory Contents

Programs used for loading control memory contents are typically dictated by the type of equipment available and the amount of convenience desired. The only requirement is that the end results allow the 6 steps above to be performed. For example, one method developed by the ElectroScience Laboratory employs, an HP 2115A computer with a high speed paper tape reader, a Tally high speed punch, an AMPEX magnetic tape drive and standard teletype. The modem loader program may be loaded from mag tape or paper tape. Control memory contents are kept on paper tape and loaded into the computer's memory for loading into the modems. This feature allows minor alteration of the modem controller program from the front panel of the HP computer. Options available from the program include reading control memory contents from a paper tape, loading control memory contents into the modem, and punching control memory contents onto paper tape with a format suitable to the 1st option. The latter two options may be performed simultaneously by inputing the proper commands via the teletype.

D. An Example of Modem Loading Program Operation

Typical operation of this program proceeds as follows:

a) After turning on the system: A magnetic tape loader program is read onto the computer from paper tape.

b) The modem loader program is read into the computer memory from magnetic tape.

c) The modem loader program is used to load the control memory contents into the computer memory from a paper tape.

d) The modem is configured as in steps 1 and 2 above. Step 3 is iniated by inputing "C" on the teletype which responds with "2C2" indicating the modem program counter has been loaded.

e) The modem is reconfigured as in step 4 above and step 5 is iniated by inputing 2 "C" characters if only the modem is to be loaded. The response is "C3C" and the computer halts indicating the loading is finished.

f) The modem is reconfigured as in step 6.

g) If the control memory contents are to be reproduced on paper tape the input in step e is "CP" and then both operations (loading and punching control memory contents) proceed simultaneously.

h) If additional modems are to be loaded with the same program or if the computer memory has not been altered since the last time the program was used the procedure is started at step d after the program is reinitiated from the front panel of the HP computer.

APPENDIX IV
CALCULATION OF ROUND TRIP DELAY

The round trip delay is calculated in terms of integer slots using the slot times shown below. The octal value of this delay is entered into location 60_8 of the data memory. The remaining fraction of a slot is converted in terms of shifts, and the octal value entered into location 61_8 (initial value of range counter) of the data memory. The delay select switch is placed in D_1 position and depressing the fine range acquisition switch causes the modem to assume a correct slot count from location 60_8 and proceed to fine range acquisition using the approximate information stored in location 61_8. The coarse range subsystem is inoperative when the modem is configured to establish HRF. The fine range acquisition mode is the only means for establishing proper transmitter timing.

HRF	LRF
128 subframes/frame	16 subframes/frame
82 slots/subframe	32 slots/subframe
146Δ (chips)/slot	146Δ (chips)/slot
Δ/4 range counter increments	Δ/32 range counter increment
Frame = 0.426 sec	Frame = 0.426 sec
Subframe = 3.33×10^{-3} sec	Subframe = 2.66×10^{-2} sec
Slot = 1.04×10^{-4} sec	Slot = 8.33×10^{-4} sec
Δ = 7.134×10^{-7} sec	Δ = 5.707×10^{-6} sec
Range counter 584 counts/slot	Range counter 4672 counts/slot
(one count = 1.78×10^{-7} sec)	(one count = 1.78×10^{-7} sec)

Example

Assume round trip range to satellite is 44,000 miles

HRF

Round trip delay 0.236559 sec.
Round trip delay 2270.967 slots
Enter 04336_8 into location 60_8 (coarse range)
(.967)(584) = 564 counts on range counter
Enter 01064_8 into location 61_8 (fine range)

LRF

Round trip delay 0.236559 sec
Round trip delay 283.871 slots
Enter 00433_8 into location 60_8 (coarse range)
(.871)(4672) = 4069 on range counter
Enter 07745_8 into location 61_8 (fine range)

APPENDIX V
RADC/OSU TDMA MODEM
TEST PROCEDURES

1.0 OVERVIEW

Because of the numerous capabilities and operating modes to be provided, the testing of even one modem to obtain quantitative data which would fully characterize its performance will be time-consuming. However, the most important performance characteristics and the integrity of the modem design will be determinable by performing the tests described herein.

2.0 TEST EQUIPMENT

The following or comparable equipments will be utilized in performing the acceptance tests:

Item	Model Number	Manufacturer
RMS Voltmeter	3400A	Hewlett-Packard
Frequency Synthesizer	5105A/5110B	Hewlett-Packard
RF Signal Generator	8640B	Hewlett-Packard
Frequency Counter	5248M	Hewlett-Packard
Spectrum Analyzer	851B/8551B	Hewlett-Packard
Oscilloscope	7900	Tektronix
Step Attenuators; 10 dB/step	355D	Hewlett-Packard
Step Attenuators; 1 dB/step	355C	Hewlett-Packard
IF Amplifier; 70 MHz	ET70-10	RHG
Hybrid Power Dividers	PD20-55	Merrimac
Bit Error Rate Tester	901	II Communications
Teleprinter	150KSR	MITE

3.0 GENERAL TEST CONDITIONS

The tests will be performed under prevailing laboratory conditions after the modems and all test equipments have been "on" for at least thirty minutes.

4.0 FUNCTIONAL-INTEGRITY TESTS

4.1 Verify that the modems perform all functions to be delineated in the intended manner when they are configured to establish the HRF.

4.1.1 Configure all modems to establish the designated format. Check the amplitudes and frequencies of appropriate signals within the analog subsystems of each modem and align circuits as appropriate. Verify that each digital phase modulator operates properly when the applicable modem is successively enabled to operate in the 2ϕ and 4ϕ PN spectrum-spreading modes. Verify that the AFC and AGC circuits within each modem operate properly.

4.1.2 Configure two modems to simulate a two-user network as described in the remainder of this subsection. Utilize a hybrid power "divider" to combine the 70 MHz transmit signals to be generated by the two modems and a second hybrid power divider to form two essentially-identical 70 MHz transmit sum signals. One of these latter signals is to be utilized for monitoring purposes only. Interconnect a 10 dB/step attenuator and a 1 dB/step attenuator, and apply the "other" 70 MHz transmit sum signal to one of those attenuators. Subsequently, the two attenuators will be designated as the signal attenuator for brevity. Interconnect a 70 MHz, 10 MHz bandwidth, high-gain IF amplifier, a 10 dB/step attenuator, and a 1 dB/step attenuator as appropriate for generating a variable-level noise voltage. The latter two attenuators will be designated as the noise attenuator. Utilize hybrid power dividers to combine the attenuated 70 MHz transmit sum signal with the variable-level (attenuated) noise voltage and to divide the combined signals into two composite "received" signals. Apply one of the latter signals to the 70 MHz input jack on each of the two modems.

Position the modem configuration switches so that the address of one modem is 10_2, the address of the second modem is 11_2, both modems operate in conjunction with network controller 01_2, neither modem operates as a network control terminal modem, and both modems operate in the 4ϕ PN spectrum-spreading mode. Position all modem test switches as appropriate for normal operation. For each modem, place the REACQ/PAUSE and TX CLK/OFF switches in the PAUSE and OFF positions, respectively, and depress the MSTR CLR momentary switch. Utilize an oscilloscope to monitor the 70 MHz transmit sum signal and successively enable each modem to generate a network clock signal (NCS) by placing the TX CLK/OFF switch on the applicable modem in the TX CLK position. Equalize

the amplitudes of the sequentially-generated NCS's by adjusting the HIGH TX potentiometer within the appropriate modem; that potentiometer is accessible for adjustment purposes from the front panel.

Set the modem IF receiver gains at their maximum values by rotating the GAIN potentiometers to their full clockwise positions, and set the signal attenuator to introduce maximum attenuation. Adjust the noise voltage attenuator so that the noise level meter on the modem with the smallest maximum gain indicates approximately 0.7. Decrease the modem gains so that both noise level meters indicate approximately 0.4. Set the signal level attenuator at 40 dB and enable the transmission of a NCS from one (and only one) modem. The modem which generates the NCS is hereafter designated as the auxiliary modem, and the other modem is designated as the modem under test. Place the REACQ/PAUSE switch on each modem in the REACQ position. After the clock-tracking loops have acquired the NCS, observe the contents of data memory location 256_8 within each modem and adjust the signal attenuator so that the observed data words have values nominally equal to 2000_8. Temporarily increase the noise voltage attenuator by at least 30 dB and adjust the modem gains so that data memory location 256_8 within each modem contains 2000_8. Return the noise voltage attenuator to its previous setting. This procedure establishes a received-signal power to noise density ratio which is approximately equal to the design value.

Set the amplitude of the signal to be transmitted from the modem under test while coarse-range acquisition is to be effected at one-third of the NCS amplitude by 1) positioning the modem test switches so that a continuous low-level signal is transmitted from the modem under test, 2) monitoring the 70 MHz transmit signal, and 3) suitably adjusting the LOW TX potentiometer. Reposition the test switches to inhibit the continuous transmission of a low-level signal.

4.1.3 Verify that the modem under test reliably performs the following functions several times in succession:

- NCS acquisition and tracking following depression of the MSTR CLR switch,
- Range pulse acquisition and tracking following depression of the FN RNG ACQ mementary switch with the DEL SEL switch in the D1 position,
- Short-cycle and full-cycle clock-loop (NCS) reacquisition procedures, in sequence, following a temporary removal of the 70 MHz input signal from the modem under test,
- Automatic range-loop reacquisition following a clock-loop reacquisition,
- Proper enabling of the teleprinter and 2400 bps I/O devices to operate in conjunction with manually-set time ordered channel assignments (TOCA's),
- Intermodem linking following the manual-enabling of suitable TOCA's and the initiation of appropriate link requests,

- Proper utilization of TOCA's to convey data between teleprinters and between bit error rate testers (BERT's) at a 2400 bps rate following the establishment of applicable links,
- Automatic termination of links following depression of the applicable CLR mementary switches,
- Relinquishment of TOCA's following link terminations and depression of the applicable REL ASGN momentary switches.

4.1.4 Enable the modem under test to operate as a network control terminal modem by suitably positioning the appropriate configuration switch and verify that functions unique to network control terminal modems are performed properly.

4.1.4.1 Initiate the transmission of a channel assignment request from the modem under test by suitably positioning appropriate switches and depressing the appropriate REQ ASGN momentary switch.

4.1.4.2 Simulate the transfer of a corresponding channel allocation control word from an external network control terminal minicomputer to the modem under test by manually-entering suitable data into appropriate data memory locations. Then, manually-set the software flag which indicates that a control word has been transferred by entering suitable data into the data memory location where the flag is stored.

4.1.4.3 Determine that the modem under test transmits and subsequently receives the control word in the applicable LLL slots, and that utilization of the TOCA designated by the channel allocation control word is automatically enabled.

4.1.4.4 Utilize procedure 4.1.4.2 to initiate the transmission of a channel relinquishment-request control word and verify that the applicable REL ASG lamp becomes lit. Release the assignment by depressing the applicable REL ASGN momentary switch.

4.1.4.5 Inhibit the modem under test from operating as a network control terminal modem by suitably repositioning the applicable configuration switch.

4.1.5 Place the TX CLK/OFF switches on the modem under test and the auxiliary modem in the TX CLK and OFF positions, respectively, and redesignate the modems as the auxiliary modem and the modem under test, respectively. Subject the "new" modem under test to tests 4.1.3 through 4.1.4.5.

4.1.6 Configure the third modem to operate in conjunction with either of the modems tested to this point as delineated in 4.1.2 and in a manner which results in the third modem being the new

modem under test. Subject the third modem to tests 4.1.3 through 4.1.4.5.

4.2 Verify that the modems perform all functions to be delineated in the intended manner when they are configured to establish the LRF.

4.2.1 Repeat tests 4.1.1 through 4.1.6 but with the modems configured to establish the LRF and with the following function added to the list of functions delineated in 4.1.3:

- Coarse range and fine range acquisition, in sequence, following the loading of data memory location 56_8 with 4, placement of the DEL SEL switch in the D1 position, and depression of the CRS RNG ACQ momentary switch.

5.0 PERFORMANCE TESTS

5.1 With the modems configured to establish the LRF, obtain bit error probability performance data suitable for assessing implementation effectiveness.

5.1.1 Determine the linearity and bandpass characteristics of the IF monitor circuit within one modem -- the modem under test -- to establish a basis for accurately determining bit energy to single-sided noise density ratios.

5.1.1.1 Configure two modems as delineated in 4.1.2. Then, position applicable test switches so that CW local oscillator signals are applied continuously to the correlation processor subsystem in the modem under test and the AFC circuit within that modem is inhibited from operating. Remove the 70 MHz transmit sum signal from the input to the signal attenuator and connect an RMS voltmeter to the 10.7 MHz IF monitor circuit output jack on the rear panel of the modem under test. For each of an appropriate number of noise-voltage attenuator settings, measure the rms amplitude of the noise voltage present at the output of the IF monitor circuit. On completing these measurements, reposition the noise voltage attenuator to its previous setting.

From the measured data, determine the rms amplitude of the monitored noise voltage for which the deviation from a linear amplitude response is nominally equal to 0.1 dB. Subsequently, maintain the monitored noise voltage smaller than that value when a noise level is being measured by suitably setting the noise voltage attenuator.

5.1.1.2 Remove the unattenuated noise voltage from the input to the noise voltage attenuator and reapply the 70 MHz transmit sum signal to the input of the signal attenuator. Enable the transmission of a CW 70 MHz signal from the auxiliary modem by suitably positioning applicable test switches within that modem. For each of an appropriate number of signal attenuator settings, measure the rms value of the 10.7 MHz signal present at the IF monitor circuit output.

From the measured data, determine the rms amplitude of the monitored signal for which the deviation from a linear amplitude response is nominally equal to 0.1 dB. Subsequently, maintain the monitored signal voltage smaller than that value by suitably setting the signal attenuator.

5.1.1.3 Set the signal attenuator to the smallest attenuation setting consistent with the constraint delineated in 5.1.1.2. Remove the 10.7 MHz jumper cable from the rear of the auxiliary modem and apply a nominal 1 v peak to peak, 10.7 MHz CW signal from a frequency synthesizer to the 10.7 MHz input jack. Determine the bandpass (amplitude) response characteristic of the IF monitor circuit by varying the frequency of the nominal 10.7 MHz signal over the passband in 50 Hz steps and measuring the amplitude of the IF monitor circuit output signal following each change in frequency. Note that the frequencies of the transmit-sum and IF monitor output signals will decrease by an amount Δf when the frequency of the nominal 10.7 MHz signal applied to the auxiliary modem is increased by an amount Δf. Utilize the measured data to calculate the noise bandwidth, B_n, of the IF monitor circuit.

5.1.1.4 Subsequently, employ the following expression to determine bit energy to single-sided noise density ratios: $(E_b/N_o)_{dB} = (P_s)_{dB} - (P_n)_{dB} + (B_n)_{dB} + (T_b)_{dB}$ where $(x)_{dB} = 10 \log_{10} x$, P_s represents the power contained in the IF monitor circuit output signal when the test switches and signal attenuator are suitably configured, P_n represents the power contained in the noise voltage present at the IF monitor circuit output jack when the test switches and noise attenuator are suitably configured, and T_b represents the duration of the data symbols actually received (not the reciprocal of the average data rate).

5.1.2 Reconfigure the two modems as delineated in 4.1.2 so that the modem under test in 5.1.1.1 remains the modem under test. Configure a BERT to operate in conjunction with the modem under test at a 2400 bps rate. Enable the utilization of a long bit length (LBL), simplex, 2400 bps TOCA by manipulating switches on the vocoder control panel of the modem under test as follows: 1) place the DPLX/SMPLX switch in the SMPLX position, 2) place both the TX and RCV switches in the LBIT positions, 3) position

the lever switches comprising the four character switch register to read 40_8, and 4) depress the LCL CNTL momentary switch. Place the applicable 2400 bps TX/RCV switch on the auxiliary control panel to the TX position. Enable the modem under test to operate in a "loop" mode by placing the DPLX/SMPLX switch in the DPLX position; otherwise, data received by the modem in the TOCA will not be output to the BERT.

5.1.3 Determine the bit error probability (BEP) performance of the modem under test for the E_b/N_o values and operating modes delineated.

5.1.3.1 Utilize the IF monitor circuit to determine the value of E_b/N_o as delineated in 5.1.1.4 and adjust the noise voltage level to establish an E_b/N_o of approximately 10 dB, if necessary. Reestablish the "normal" test configuration on completing this procedure.

5.1.3.2 Artificially constrain the differential detector bit timing error at a negligibly-small value by 1) placing the TX CLK/OFF switches on the auxiliary modem and the modem under test in the OFF and TX CLK positions, respectively, 2) temporarily increasing the noise voltage attenuator setting by at least 30 dB, 3) loading data memory location 376_8 within the modem under test with "all zeroes," and 4) returning the noise voltage attenuator to its original setting. Inhibit the AFC and AGC circuits within the modem under test from operating by suitably positioning the appropriate test switch and the AGC mode-control switch on the baseband module.

5.1.3.3 Utilize the BERT to determine the BEP for the E_b/N_o value established in 5.1.3.1. Then, successively increase the signal attenuator setting in one dB steps and determine the BEP following each change in setting until BEPs have been measured for five E_b/N_o values. Reposition the signal attenuator setting to reestablish a nominal 10 dB value for E_b/N_o on completing these measurements.

5.1.3.4 Enable the modems to operate in the 2ϕ PN spectrum spreading mode by suitably positioning the 2ϕ/4ϕ test switches.

5.1.3.5 Successively determine BEPs for nominal E_b/N_o values of 9, 8, and 7 dB.

5.1.3.6 Verify from the data obtained in 5.1.3.3 and 5.1.3.5 that the degradations from ideal performance, i.e., the amounts by which the E_b/N_o values required to achieve given BEPs exceed the E_b/N_o values which would be required to achieve those BEPs if the detector were to be ideally implemented, are equal to or less than 0.5 dB for the operating modes established in 5.1.3.2 and 5.1.3.4.

5.1.3.7 Load data memory location 376_8 within the modem under test with 177777_8, and enable operation of the AFC and AGC

circuits within that modem by suitably positioning the appropriate switches. Repeat test procedure 5.1.3.5. Enable the modems to operate in the 4ϕ PN spectrum-spreading mode and recalibrate as delineated in 5.1.3.1. Repeat test procedure 5.1.3.3. Verify from the data obtained that the degradations from ideal performance for the operating modes established do not exceed 0.7 dB.

5.1.3.8 Position the TX CLK/OFF switches on the modem under test and the auxiliary modem to the OFF and TX CLK positions, respectively. Repeat test procedures 5.1.3.3 through 5.1.3.5. Verify that the degradations from ideal performance for the operating modes established do not exceed 1.1 dB.

5.1.3.9 Enable the modems to operate in the 4ϕ PN spectrum-spreading mode. Depress the REL ASGN momentary switch on the vocoder control panel of the modem under test. Enable the utilization of a short bit length (SBL), simplex 2400 bps TOCA by the modem under test by following the procedures delineated in 5.1.2 but with the TX and RCV switches in the SBIT positions rather than the LBIT positions. Repeat tests 5.1.3.1 and 5.1.3.5. Verify that the degradation from ideal performance does not exceed 0.9 dB.

APPENDIX VI
TEST RESULTS WITH THE LES-6 SATELLITE

1. INTRODUCTION

Four time division multiple access (TDMA) satellite communication modulators/demodulators (modems) were developed for the Rome Air Development Center (RADC) by The Ohio State University (OSU) ElectroScience Laboratory under Air Force Contract F30602-72-C-0162 [1]. Two of these modems were operated in conjunction with equipments at the OSU Satellite Communication Facility to establish "loop" links via Lincoln (Laboratory) Experimental Satellite number six (LES-6) and data which partially characterizes their performance were obtained. Those data are presented herein and compared with results projected from bench data obtained previously. The tests were conducted with the assistance of Messrs. Stuart Talbot and Anthony Greci of RADC. Their contributions are gratefully acknowledged.

2. OVERVIEW

Exclusive authorizations to utilize LES-6 for experimental purposes were arranged by the project monitor, Mr. Stuart Talbot, as follows:

DATES	TIME INTERVALS
14 April 1975	0600-1000 Z
18 April 1975	0600-1000 Z
25 April 1975	2100-0100 Z
26 April 1975	1200-1600 Z
29 April 1975	2100-0100 Z
30 April 1975	2100-0100 Z

The UHF equipments utilized to establish links were "debugged" and selected characteristics of LES-6 were determined during the first few test intervals. Subsequently, two of the prototype modems were operated in conjunction with the UHF terminal and LES-6 to establish "loop" links, and appropriate tests were conducted to obtain data descriptive of modem performance.

3. LINK CHARACTERISTICS

A basis for interpreting modem test data was established by transmitting a linearly-polarized cw 302.7 MHz signal to LES-6 at the highest level possible with the equipments utilized -- approximately 36 dBw, receiving the associated down-link signal, and processing the received signal to determine its amplitude and spectral characteristics. The received signal was successively down-converted to a 70 MHz IF, amplified, bandpass filtered to restrict its spectral width to approximately 500 MHz --

the nominal bandwidth of the LES-6 transponder, and applied to the input of a Hewlett Packard model 851B/8551B spectrum analyzer. A representation of the signal spectrum is shown in Figure 1. This data indicates that the composite signal (effectively) present at the analyzer input consisted of 1) thermal noises generated by the receiver and analyzer, 2) a narrow-band "desired" signal having a frequency essentially equal to the center frequency of the LES-6 transmit subsystem, 3) a narrow-band undesired signal having a frequency approximately 180 KHz greater than the midband frequency and an amplitude only two to three decibels smaller than the amplitude of the desired signal, and 4) multiple undesired signals having amplitudes approximately twelve decibels below the desired-signal amplitude. The spectra of the noise voltages and the high-level undesired signal were essentially invariant with time irrespective of the effective power radiated on the up-link. The high-level desired signal was definitely radiated from LES-6 as moving the antenna boresight axis from the LES-6 pointing angles resulted in the amplitude of the associated signal present at the receiver output decreasing in accord with the pattern characteristics of the receiving antenna. Also, a spurious signal was received concurrently at the government facility from which the utilization of LES-6 was being coordinated. Fortunately, nulls existed in the spectra of the modem-generated signals at frequencies displaced from midband by integer multiples of plus and minus 175.2 KHz. As a result, the high-level undesired down-link signal was not expected to -- and apparently did not -- significantly degrade modem performance.

Unlike the high-level undesired signal, the lower-level undesired signals received exhibited highly dynamic amplitude and spectral characteristics. On occasion, a frequency-hopped signal was present on the down-link which had an amplitude only a few decibels smaller than the amplitude of the highest-level down-link desired signal received. As to be addressed subsequently, the lower-level undesired signals undoubtedly degraded the bit error probability performance of the modems. Thus, quantitative (statistical) data descriptive of their characteristics would preferably have been obtained. However, the expenditure of time and other resources that would have been required to characterize adequately the lower-level undesired signals was considered to be unwarranted.

The amplitude characteristics of the desired down-link signal received when a cw signal was transmitted on the up-link were determined by utilizing a multiple down-conversion receiver to generate a 455 KHz IF signal having a spectral width of approximately 5 KHz from the 70 MHz IF received signal, employing a Hewlett Packard model 3400 A RMS voltmeter to measure the amplitude of the 455 KHz IF signal, and utilizing a strip chart recorder to record the voltmeter response. A section of the recorded data is reproduced in Figure 2. This data shows that the signal amplitude varied over a 5.7 dB range in a periodic fashion every 6.4 seconds. Since LES-6 is spin stabilized and the spin period equalled 7.353 seconds at some time prior to February 1971 [2], the period of the down-link signal amplitude variations was probably equal to the LES-6 spin period. Quite likely, the amplitude fluctuations were due to a failure or failures in the LES-6 electrically-despun UHF transmit and/or receiving arrays.

4. TDMA MODEM LOOP-LINK TESTS

The two TDMA modems which were implemented with random access control memories, modems #01 and #02, were employed to establish the lower-rate (TDMA signaling) format (LRF) via LES-6. Since only one thirty-foot diameter antenna at the OSU Satellite Communication Facility can be configured to operate in the UHF band, the tests were necessarily performed by operating both modems in conjunction with the same terminal, i.e., with one transmitter and one receiver. One modem was normally enabled to transmit the network clock signal (NCS) required to establish the TDMA signaling format during the tests. Thus, the transmit time base (clock) maintained within only one modem -- the modem not enabled to transmit the NCS at a given time -- was controlled on a closed-loop basis. Since the modems were colocated, the simultaneous transmission of signals from them was never required.

The functional integrity of the modems was evaluated by establishing conditions likely to exist in an operational system, executing an operating procedure which does not depend on a priori knowledge of the operating conditions for each modem on an indidivual basis, and observing the modem responses. The unfavorable link conditions described in Section 3 nothwithstanding, all overhead functions required to establish and maintain a TDMA satellite communication network [1], e.g., time base acquisition, time base tracking, and intermodem linking functions, were repeatedly performed in an effective manner whenever the maximum bit energy to noise density ratio associated with each signal received was nominally equal to or greater than the constant bit energy to noise density ratio value on which the modem design was based: 10.6 dB. Moreover, mechanisms incorporated in the modems to prevent anomalous operation whenever the amplitude of the received signal assumes an unacceptably small value [1] were shown to be highly effective. A teleprinter was operated in conjunction with one modem in an "echo" mode during the functional tests to verify that all overhead functions were, in fact, being performed properly.

On completing the functional tests described, bit error probability data were obtained by establishing a 2400 bps time-ordered simplex link between the two TDMA modems via LES-6 and appropriately utilizing an II Corporation model 901 bit error rate tester (BERT). Worst case conditions were established by configuring modem #01 to transmit the NCS and modem #02 to transmit a symbol stream generated by the BERT, i.e., data was transmitted from the modem in which the transmit time base was maintained by a sampled-data delay-lock "range-tracking" loop. Both modems were enabled to operate in the four-phase (4ϕ) spectrum spreading mode* [1]. The BERT

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*Within each modem, data symbols to be transmitted are differentially encoded and the encoded symbols are impressed as biphase modulation on either a biphase or a quadraphase modulated (spread spectrum) local oscillator signal depending on the position of a 2ϕ/4ϕ mode control switch. The sprectrum spreading factor equals sixteen for a long bit length (LBL) time ordered channel: the type of channel utilized during the tests performed.

was configured to generate repetitively a length-63 pseudo-noise (PN) sequence in synchronism with the 2400 Hz transmit clock generated by modem #02 and to receive data from modem #01 in synchronism with the 2400 Hz receive clock generated by the latter modem. Data obtained from the tests are shown along with projected performance curves in Figure 3. The means employed to generate the projected results are described after a suitable basis for discussion is established in the following paragraph.

The bit error probability performance of the TDMA modems was determined previously by performing bench tests as described in the applicable acceptance test procedures; data obtained from those tests are shown in Figure 4. The worst-case data shown in this figure were obtained by testing two modems configured essentially as described in the foregoing paragraph but with the modems interconnected directly rather than via a relay satellite. These data are displaced from the ideal bit error probability performance curve by only 0.8 dB. However, the effects of large round-trip propagation delays, propagation phenomena, transponder nonlinearities, and relative satellite/terminal motion are not reflected in the best test data. The link tests performed were originally intended, in part, to provide a measure of the incremental degradation in modem performance due to "normal" link and transponder imperfections when the modems are operated in the intended manner. The test data actually obtained reflect the effects of abnormal variations in the effective down-link gain and interference in addition to the effects of normal imperfections. Nonetheless, important modem characteristics are discernible from the data obtained as discussed in the following paragraph.

The period associated with the observed down-link gain fluctuations spanned a relatively large number of (approximately 15) TDMA signaling frames. Consequently, a first order approximation to the modem bit error probability performance attainable in the absence of interference and normal link and transponder imperfections can be obtained by modeling the loop-link gain fluctuations in a piecewise-constant fashion as shown in Figure 5 and employing the following expression to calculate the error probability:*

$$(1)\quad P_{E_{p1}} \doteq \frac{12.5}{21.5}\, P_{E3}\left|_{\frac{E_b}{N_o}=\frac{P_{r1}T_b}{N_o}} + \frac{(3+2)}{21.5}\, P_{E3}\right|_{\frac{E_b}{N_o}=\frac{P_{r2}T_b}{N_o}} + \frac{4}{21.5}\, P_{E3}\left|_{\frac{E_b}{N_o}=\frac{P_{r3}T_b}{N_o}}\right.$$

*For the operating mode utilized during the LES-6 tests, a constant P_r/N_o value of 51 dB·Hz results in an E_b/N_o value of 10.6 dB: the design value.

In this expression, P_{r1}, P_{r2}, and P_{r3} represent signal powers which are defined in Figure 5 and $P_{E3}(E_b/N_o)$ represents the bit error probability performance of the modems when they are interconnected directly and operated in the worst-case configuration (see Figure 4). The dependence of $P_{E_{p1}}$ on P_{r1}/N_o is shown graphically in Figure 3. Two of the test data points shown in Figure 3 are very close to the $P_{E_{p1}}$ curve, but the measured bit error probability for P_{r1}/N_o equal to 55.8 dB · Hz is approximately an order of magnitude larger than the value determined from Equation (1). The discrepancy was undoubtably caused by the lower-level undesired signals present on the down-link (see Sec. 3).

No basis exists for accurately estimating the extent to which the bit error probability performance would necessarily have been degraded by interference during the tests since large variations occurred in the down-link desired-signal to interference power ratio and in the spectra of the interfering signals which were not characterized quantitatively. The former variations were due, in part, to changes which were made in the level of the desired up-link signal incident on LES-6 to alter the value of P_{r1}/N_o. These changes were made by offsetting the antenna boresight axis from the direction of LES-6 rather than by varying the up-link ERP*. As a result, a given change (reduction) in P_{r1}/N_o resulted from changes in both the transmit and receive antenna gains (as would changes which would occur at an airborne terminal in an operational system). Notwithstanding the fact that the signal to interference ratio was not constant during the tests, the bit error probability performance attainable under the interference conditions which existed can easily be estimated if it is presumed 1) that interference resulted in the occurrence of four detection errors for every 100,000 data symbols detected, on the average, irrespective of the value of P_{r1}/N_o and 2) that the errors due to interference and other causes were additive. These presumptions and Equation (1) were jointly utilized to generate the dashed curve shown in Figure 3. This curve, although not strictly applicable, indicates that the modem performance probably did not differ significantly from the best performance attainable under the conditions which existed during the tests.

It is important to note that, had the modems not been implemented to effect spectrum spreading, their bit error probability performance would have been limited by interference for all three values of P_{r1}/N_o for which test data was obtained and the bit error probability would have leveled-off, or nearly so, at a value much larger than the actual value of approximately $4 \cdot 10^{-5}$. Thus, although the processing gain provided by the modems was not adequate to prevent interference present during the tests from degrading modem performance for larger values of P_{r1}/N_o, the modem

*Thermal noise could also have been added to the received signal to vary P_{r1}/N_o. However, this approach would have resulted in more favorable operating conditions and an attendant reduction in the creditability of the data obtained.

performance during the LES-6 tests would probably have been totally unacceptable had the modems not been implemented to effect spectrum spreading*.

5. CONCLUSIONS

The results obtained by testing the prototype RADC/OSU TDMA modems in conjunction with LES-6 indicate that modem performance does not depart significantly from the attainable performance -- even when the modems are operated under adverse conditions. Although not intended by design, the tests performed provide significant insight into the performance which might be expected of a TDMA system wherein some terminals would be airborne (if the terminals were to be equipped with modems similar to the prototype modems). Such a system would experience interference not unlike the interference present during the tests completed. Also, under unfavorable conditions, the amplitude of the signal which would be received by a given airborne terminal would vary over at least a six decibel range as a result of imperfections in the pattern of the receiving antenna and multipath propagation. The temporal structures of those variations and the variations which occurred during the tests completed would, of course, differ significantly. Nonetheless, the test results obtained indicate that modems similar to the prototype modems should be utilizable to implement practical and effective TDMA satellite communication systems werein some terminals would be airborne, in addition to systems which would normally operate under more favorable conditions.

*Bench test results have been obtained which show that the modems provide an effective processing gain of approximately five decibels when data are conveyed between them via long bit length time ordered channels -- when the signal spectra are spread by a factor of sixteen -- and when cw interfering signals are present at their inputs.

REFERENCES

[1] R. J. Huff, "Multifunction TDMA Techniques," Report 3364-3, August 1974, The Ohio State University ElectroScience Laboratory, Department of Electrical Engineering; prepared under Contract F30602-72-C-0162 for Rome Air Development Center. (RADC-TR-74-327) (AD/A 004196)

[2] I. L. Lebow, K. L. Jordan, Jr., P. R. Drouilet, Jr., "Satellite Communications to Mobile Platforms," Proc. IEEE, Vol. 59, No. 2, February 1971, pp. 139-159.

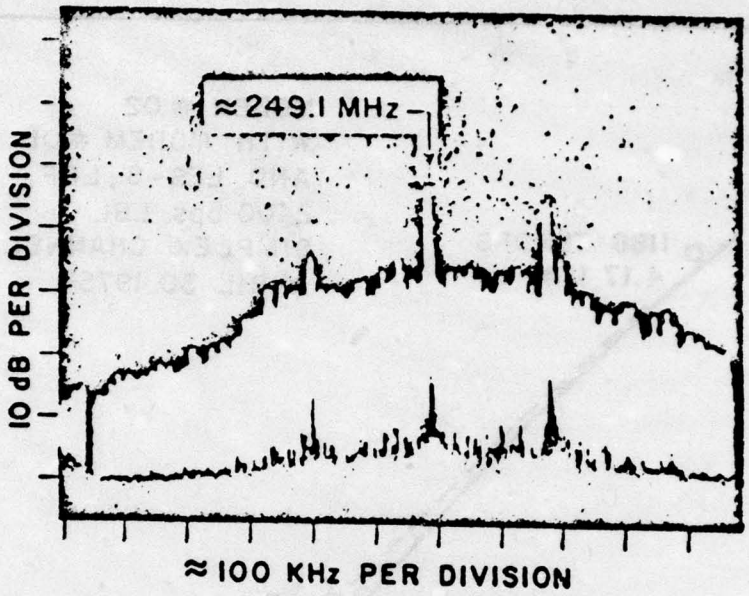

Figure 1. Nominal spectrum of the signal received from LES-6 when a linearly-polarized cw 302.7 MHz signal was transmitted on the up-link at an ERP of approximately 36 dBw.

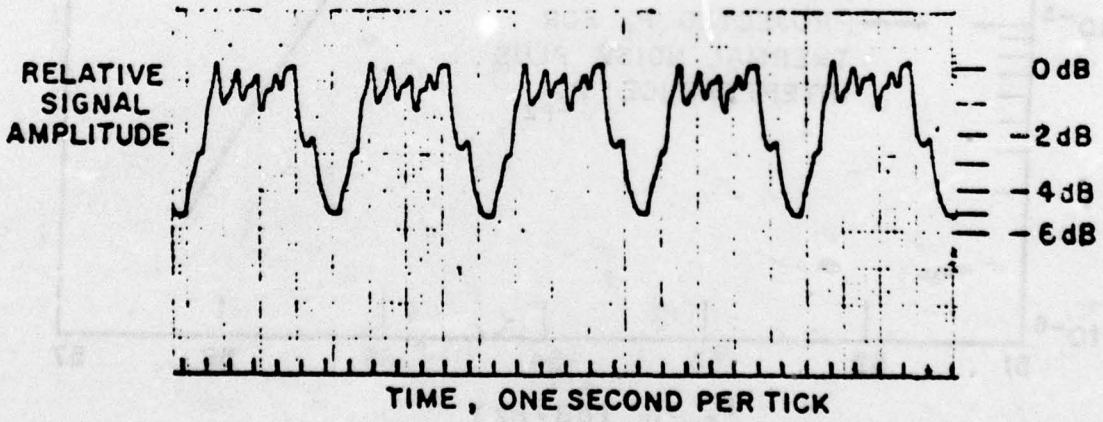

Figure 2. Relative amplitude of the desired signal received from LES-6 versus time when a linearly-polarized cw 302.7 MHz signal was transmitted on the up-link at an ERP of approximately 36 dBw.

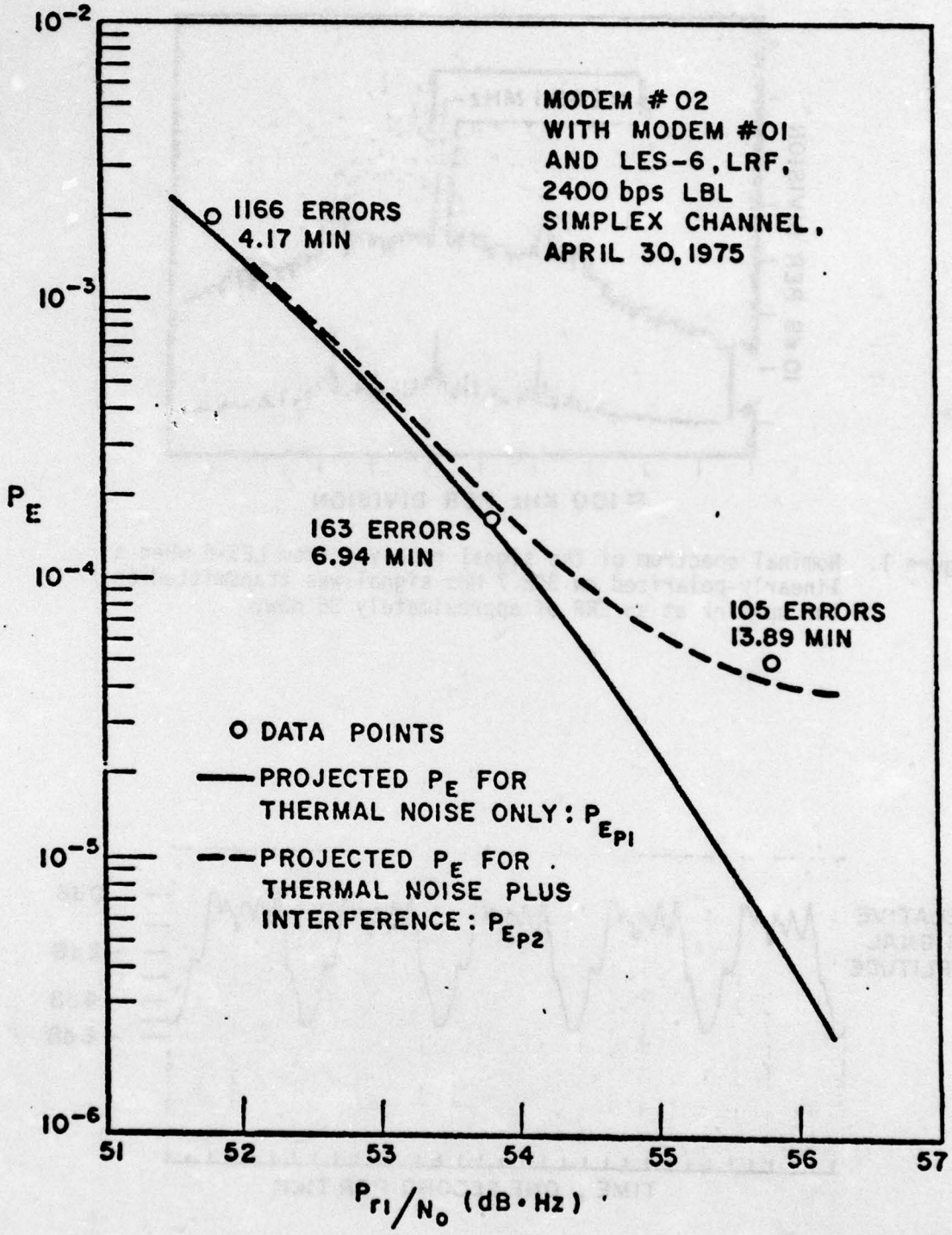

Figure 3. LES-6 bit error probability data and projected results.

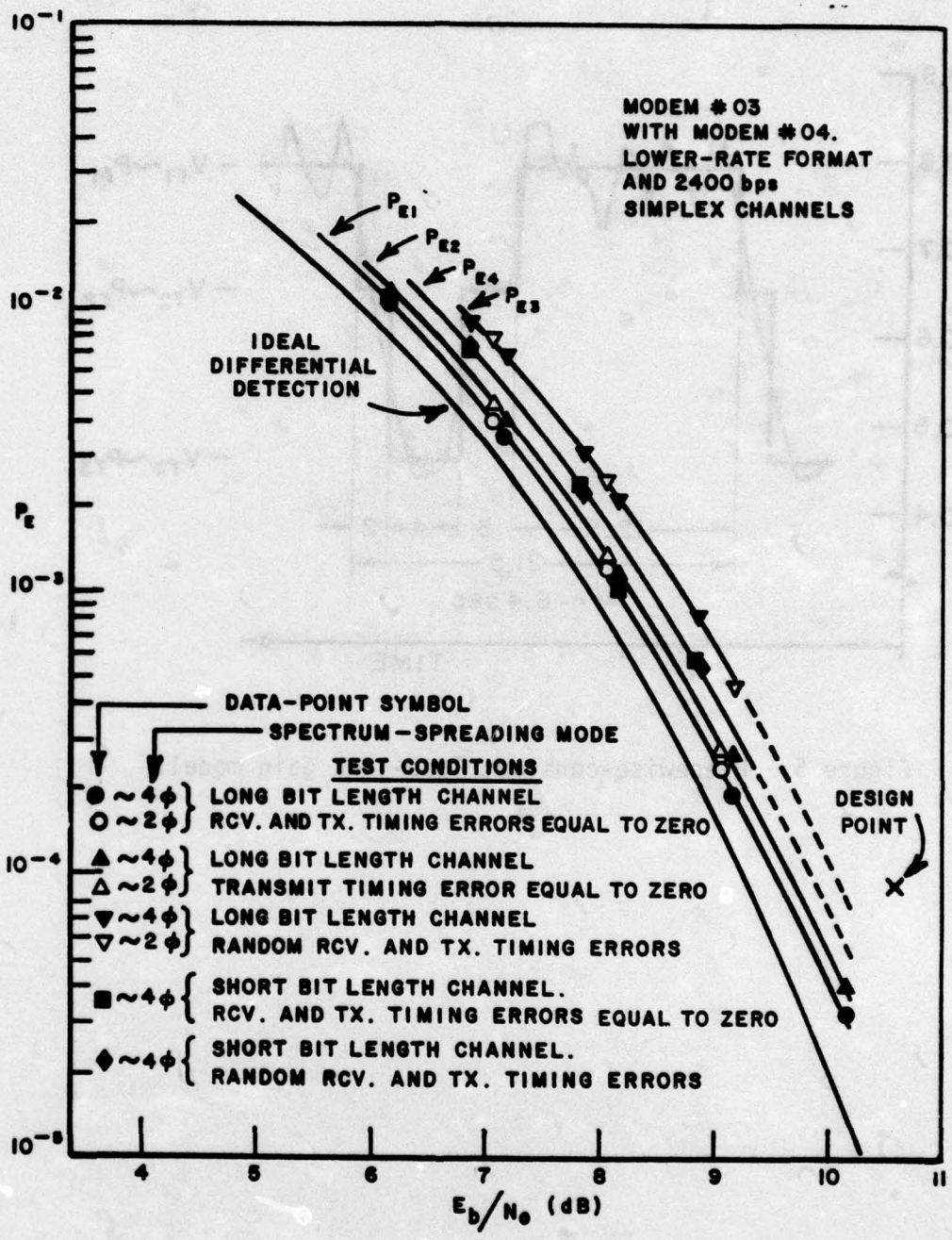

Figure 4. Bench test bit error probability data and the ideal differential detection performance curve.

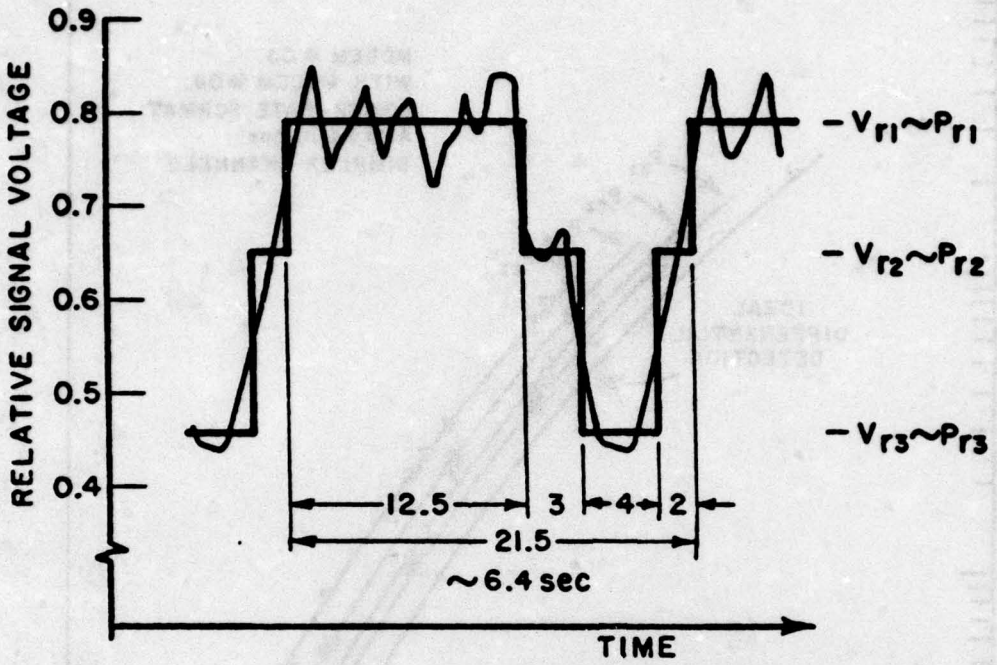

Figure 5. Piecewise-constant loop-link gain model.